STUDY OF RADIATION INDUCED INTERFACE DEFECTS AND EFFECT OF ANNEALING IN Si/ITO HETROJUNCTIONS

by

VISHWA VANDHU MISHRA

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VISHWA VANDHU MISHRA

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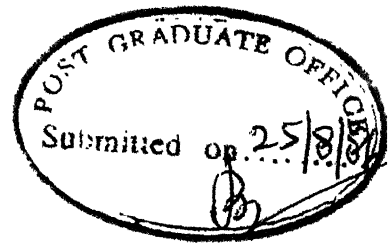

CERTIFICATE

This is to certify that the thesis entitled 'STUDY OF RADIATION INDUCED INTERFACE DEFECTS AND EFFECT OF ANNEALING IN Si/ITO HETEROJUNCTIONS' by Vishwa Vandhu Mishra is a record of work carried out under my supervision and has not been submitted elsewhere for the award of a degree.

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August, 1986

ABSTRACT

The study of interface state defects at the Si/SiO_2 interface is vital for VLSI devices. Also, with ever increasing applications of opto electronic devices, transparent conductor/silicon heterojunctions are getting useful. The present study involved evaluation of interface state density, generated due to process induced radiation damage and effect of annealing in Si/ITO heterostructures having thin (<40 Å) interfacial layer.

The samples were prepared by chemical cleaning, etching, thermally oxidising and depositing ITO film by E-beam gun, of silicon wafers. The back contacts were formed by Al metallizing. The annealing in one of the samples was carried out in forming gas (N_2/H_2) ambient at 500°C for 30 minutes. The oxide thickness was aimed at 25 Å.

Capacitance-voltage and conductance-voltage measurements were conducted. Also to consider effect of tunneling, expected in t_{ox} (25 Å) as employed here, current-voltage characteristics were also measured.

The evaluation of interface state density was done by the capacitance as well as the conductance techniques. For the conductance analysis, effect of d.c. conductance due to tunneling was considered. From the $\overline{C}^2$-Bias plots barrier heights were determined.

It has been observed, that due to annealing, the increase in barrier height has been substantially large and is 0.42 V whereas reduction in interface state density N_{is} has not been that much. A charge balance analysis at the interface shows that the reason for large increase of barrier height could be more due to reduction of fixed oxide charge Q_F (which is positive in nature) than the reduction in interface state density.

The present study involving thin t_{ox} (<40 Å) reveals that a much larger barrier height change as noticed, may be more due to reduction of fixed oxide charge Q_F than reduction of interface state charge Q_{is} or interface state density N_{is}.

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CONTENTS

CHAPTER 1

INTRODUCTION

The technological advancement of silicon integrated circuits has led to Very Large Scale Integration (VLSI) of devices, having micrometer and submicrometer elements. The VLSI systems mostly employ MOS technology for fabrication, well known for its advantages, such as device miniaturization, low device power dissipation and high yield [1]. The diminishing dimensions of MOS structures has emphasized the need for improved structural model of the silicon/silicon oxide interface. For such silicon MOS devices, having less than 100 Å thick SiO_2 insulating layer, the density of characteristic defects at the Si/SiO_2 interface has to be low. The energy states in the band gap of silicon, at the Si/SiO_2 interface of MOS structures usually cause bias shifts, generate excess leakage currents and produce flicker noise [2].

The present investigation of Si/SiO_2 interface, though based on MOS techniques, uses Transparent Conductor-Oxide-Silicon (TCOS) structures. The TCOS structures closely resemble MOS structures. The gate metal layer, such as Al or Au in MOS is being replaced by a transparent conductor which is frequently stannic oxide (SnO_2) or Indium oxide (In_2O_3).

The transparent conductors are transparent to

are conducting due to strong degeneracy. The resistivity of transparent conductors are in the range of 1×10^{-3} Ohm-cm to 1×10^{-4} Ohm-cm, and the transparency being 80% to 90%.

In opto electronic devices, where interaction of light with semi-conductor is involved, use of transparent conductors has obvious advantages. Earlier, bulk properties of transparent conductors such as transparency and conductivity were effectively applied in wind shield deicing and defogging. Later, with advancement of thin film technology and high vacuum technology, a large number of passive, as well as active applications emerged [3-6]. The passive applications, include, infrared reflectors for glass windows and incandescent lamps, anti-static coatings for instrument panels, protective and wear resistant coatings for glass containers, low temperature secondary thermometers, thin film resistors, anti reflection coatings and reflector absorber tandem for photo thermal conversion. On the other hand, active applications in liquid crystal display (LCD), light emitting diode (LED), imaging tubes, photo detectors, charge coupled devices (CCD) and solar-cells are to name a few.

The solar cells, consisting of In_2O_3, a transparent conductor and Si heterojunction, with thin ($\simeq 20$ Å) SiO_2 interfacial layer has distinct advantage over MOS structure as most of photons reaching the top surface of transparent conductor, can get through the transparent conductor

layer and are absorbed in the semi-conductor to create electron-hole pairs. Such solar cells have shown to possess greater than 14% efficiency [7]. Besides, layers of SnO_2 or In_2O_3 are mechanically durable being resistant to abrasion and have good adherence to Si/SiO_2 surfaces. Being oxides of metals they are chemically more stable. Their ability to form high surface barrier on semi-conductors render them useful in active optoelectronic devices, especially solar cells [8]. As to be seen in the following, transparent conductor/SiO_2/Si structures have an unique role in characterization of Si/SiO_2 interface.

Over the last two decades MOS structures have been the main tool for investigation of Si/SiO_2 interface. The admittance technique as outlined by Nicollian and Goetzberger [9] has been well established for characterization of Si/SiO_2 interface using MOS structures. Kar and Dahlke [10] extended it for thin (20-40 Å) silicon oxide interfacial layer. However in almost all cases measurements were conducted in the dark. Using semi-transparent metals in MOS, Poon and Card [11] have shown, that optical illumination extends capability of conductance technique, as it provides access to minority carrier bandgap half and thus helps to provide more meaningful characterization of silicon bandgap at the Si/SiO_2 interface. Kar et al [12], used a transparent conductor instead of a semi-transparent metal as gate electrode and successfully demonstrated its advantages and usefulness over semi-transparent metals as

following. The semi-transparent metal layer has to be thin for exploiting optical illumination technique, while deposition of thin semi-transparent metal film poses structural and chemical stability problems, a transparent conductor, such as indium tin oxide (ITO), typically 2000 Å thick is easier to deposit and is relatively superior in mechanical properties. Thus, TCOS structures offer, yet another promising and better equipped tool, for Si/SiO_2 interface investigation.

The Si/SiO_2 system possesses a number of electronic defects which give rise to fixed oxide charges, trapped charges and interface states, causing deviation from ideal characteristic of an MOS/TCOS. The fixed charges and trapped charges cause a parallel shift of capacitance-voltage characteristic and mobile alkali charges give rise to a drift. The interface states being electrically active, contribute to the capacitance of device and thus play an important role in device performance. The interface state density and its distribution over energy in the bandgap of silicon has been found to depend on the oxide thickness, for the thicknesses less than 200 Å [13].

Although nature and origin of interface defects is not yet well understood, the growth mechanism of silicon oxide and further deposition processes have great influence on creation of interface state defects. Several techniques for growing SiO_2 such as thermal oxidation [14], wet anodisation, chemical vapour deposition, and plasma anodization

[15] have been developed. Thermal oxidation is the most preferred technique. During thermal oxidation, oxidation enhanced diffusion (OED) and oxidation induced stacking faults (OSF) grow [16]. The major characteristic defect in thermally grown silicon oxide has been identified as a triply coordinated Si atom with a dangling orbital, creating interface state energy distribution over the Si bandgap [17].

Amongst the other process induced interface defects, ionizing radiations play an important role [18]. The generation of interface traps due to ionizing radiations has been correlated with Si/SiO_2 interfacial stress which depends on density of strained bonds in that region [19].

Most of the deposition techniques available for gate material deposition in an MOS/TCOS structure namely E-beam evaporation, ion plating, sputtering etc. involve energetic particles and as such create secondary particle emission. These secondary particles or X-Rays and back scattered electrons cause damage to Si/SiO_2 interface and in turn have deleterious effect on the properties of interface. When Si/SiO_2 interface is exposed to penetrating X-Ray radiations, electron-hole pairs are created. Though electrons are swept out of oxide, holes get trapped and cause oxide to get positively charged [21]. Thermally grown SiO_2 known to possess H in form of Si-H or Si-OH [22], are susceptible to ionizing radiations, and on interaction create interface states [23].

An effective way to reduce the above mentioned process induced damages, is annealing under controlled conditions [24, 25]. Although full recovery may still not be possible even under best known annealing conditions, tried so far [26].

Our interest here in this study is to demonstrate extent of radiation damage at the Si/SiO_2 interface and to note annealing effect on such damage. The samples employed are TCOS structures-ITO/nSi heterojunctions with a thin ($\simeq$ 30 Å) interfacial SiO_2, fabricated by thermally grown SiO_2 on Si and deposition of indium tin oxide (ITO; In_2O_3 90 wt. %, SnO_2 10 wt. %) by E-beam evaporation technique.

The second chapter describes in detail the Si/SiO_2 interface, the interface states, the theoretical and experimental knowledge about the nature and origin of interface states, generation and creation of interface states by thermal oxidation and ionizing radiations. Also, as to how these process induced defects could be reduced by annealing. It further deals in theory behind measurement and experimental techniques namely admittance techniques for the thin oxide which have been employed in the present study.

The third chapter provides details of fabrication of samples, the measurement set up and procedure and analysis of current-voltage, capacitance-voltage and conductance voltage data, measured on samples.

In the fourth chapter, results of the study are discussed and finally the conclusion and suggestions for further study are included.

CHAPTER 2

THE SILICON/SILICON DIOXIDE INTERFACE CHARACTERIZATION

2.1 The Silicon/Silicon Dioxide Interface

The silicon dioxide/silicon interface contains a transition region, both in terms of atom position and stoichiometry. Various charges and trap states are associated with thermally grown oxides, some of which have been identified with electronic defects in the transition region [14, 27, 28]. A charge in the oxide or transition region can induce a charge of the opposite polarity in the underlying silicon, thereby affecting the electrical characteristics of the MOS device, resulting in yield and reliability problems. Figure 2.1 shows the $Si-SiO_2$ interface and various charges associated with it [29].

The fixed oxide charge, which is positive, is located in the oxide within approximately 30 Å of the silicon layer in the transition layer. These charges are not electrically active – cannot be charged or discharged due to external bias. Hence these charges cause a parallel shift only of the capacitance-voltage characteristics along the voltage axis. The density of these charges range from $10^{10}/cm^2$ to $10^{12}/cm^2$ and depends on substrate orientation as well as oxidation and annealing conditions. These charges arise due to structural defects in the transition region. Oxide trapped charges are due to electrons or

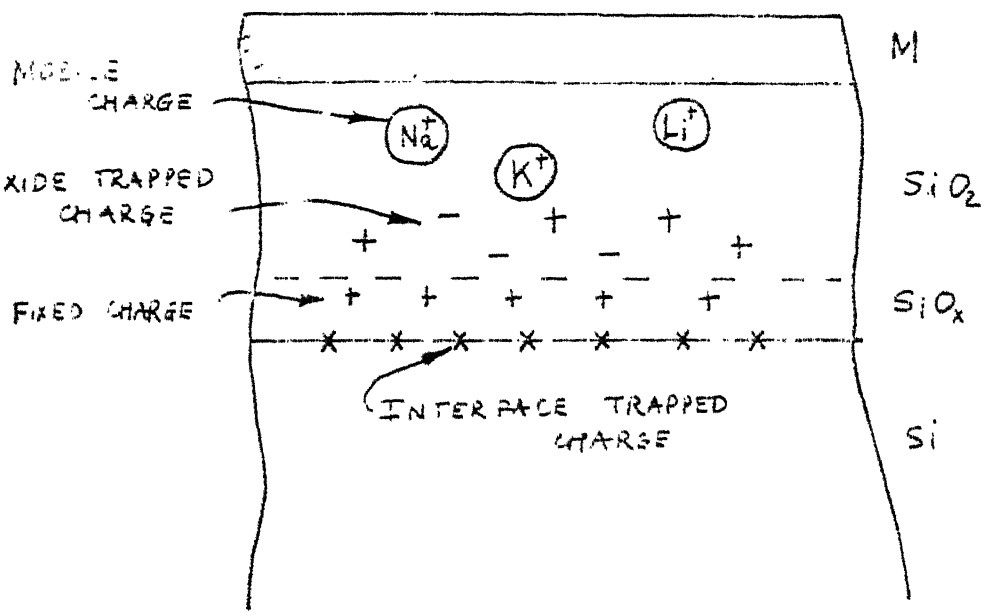


FIG. 2.1 CHARGES IN THERMALLY OXIDISED SILICON.

holes trapped in the bulk of the oxide. These charges are associated with the defects in the oxide, resulting from ionizing radiations like alpha particles and avalanche injection of carriers into the oxide. Modern processing and deposition techniques such as ion implantation, E-beam metallization, plasma or reactive ion etching, ion beam milling and E-beam or X-ray lithography used in the fabrication of VLSI circuits will also give rise to such charges. These charges can be removed by annealing [30], however subsequent processing should not use ionising radiations. The density of these charges range from 10^{9} cm^{-2} to 10^{13} cm^{-2}. Like the fixed oxide charges, the trapped charges also give rise to a shift in the capacitance-voltage characteristics.

The mobile charges are associated with alkali ions, such as sodium, potassium and lithium ions in the oxide. The alkali ions are mobile even at room temperature, when electric field is present, hence these cause drift. These ions get into the oxide mainly due to contamination in processing materials, chemicals used, ambient and handling, cleaning the furnace in chlorine ambient and gettering in phosphosilicate glass and the use of chlorine or HCl in the oxidation ambient reduces this charge, which ranges from 10^{10} cm^{-2} to 10^{12} cm^{-2}.

Located at the interface, the interface trapped charges have energy states in the silicon bandgap and can interact electrically with the underlying silicon. These charges contribute to the device capacitance and thus can

charge or discharge with applied signals. Hence an understanding of the exact source of these states, their density and their distribution over energy in the silicon bandgap is of importance. A lot of reliable data has been obtained on the interface state density and its distribution over the silicon bandgap [31, 32]. Most unannealed MOS capacitors are reported to exhibit an interface state density profile consisting of two peaked distributions, one close to the valence band maximum and the other close to the conduction band minimum overlying a concave background. The peaked distribution have been attributed to non-stoichiometry at the interface and mostly disappear on annealing leaving behind a U-shaped profile [33].

2.2 The Origin of Interface States

The surface of a semiconductor crystal interrupts the perfect periodicity of the crystal lattice. The surface atoms have neighbours on one side only and on the vacuum side the valance electrons have no partners to form covalent bonds. Each surface atom therefore has associated with it an unpaired electron, directed away from the orbit often spoken of as a 'dangling bond', it can either give up its electron and act as a donor or accept another and act as an acceptor. Also, during silicon crystal growth some oxygen (10^{17}-10^{18} atoms cm^{-3}) is incorporated interstitially in silicon lattice [34]. During thermal processing involved during fabrication, precipitation of interstitial

oxygen into Si lattice occurs [35]. Based on size and density of these precipitates, each SiO_2 molecule formed in Si lattice occupies approximately the equivalent volume of two Si atoms. Therefore each SiO_2 molecule formed in Si lattice would require either a presence of a vacancy or generation of an interstitial. Thus precipitation of oxygen is associated with extrinsic stacking faults.

The origin of interface trap generation is traced to weak SiO_2/Si bonds due to water related centers 36 . Strained Si-O bonds have also been considered for interface trap generation [37]. The mechanism is not yet well understood. Many authors believe it to be associated with release of bonded H_2 by ionizing radiations and subsequent breakage of interfacial bonds [36, 38] whereas in strained bonds model, interface traps at Si/SiO_2 interface may be generated by interaction of ionizing radiations, presence of high electric field stress, by avalanche injection or by internal photoemission.

Based on semi-empirical light bonding Hamiltonians and Green's function formulation to the electronic structures of crystalline silicon amorphous SiO_2 interface. Sakurai and Sugano [39] have concluded that the Si-Si weak bonds and Si-O weak bonds produce trap states in the upper and lower half of the bandgap respectively. The continuous distribution is explained by taking into account that the bond angles and bond lengths varying over a range give rise to states having different energies which also vary

over a range. The bonding parameters at the actual Si/SiO_2 interface can be supposed to vary because of amorphous structure and the large internal stress. On the other hand, the reduction of these states on H_2 or Cl annealing is explained as due to the changes in the state energy, caused by the bonding of H or Cl to the Si atom at the interface, which moves into the valance band and conduction band.

Experimental studies [40] using Electron Paramagnetic Resonance (EPR) have revealed a P_b center, which is a major characteristic defect of the Si/SiO_2 interface, and has been identified as a triply co-ordinated silicon atom with a dangling bond orbital aligned along (111). The energy distribution of P_b centers have two peaks one at 0.3 eV above the valence band and the other 0.8 eV above the valance band. Recently, same structures examined by EPR as well as C-V analysis, have shown that interface state profile and P_b center profile have close correlation in peak position as well as peak value of interface density. This indicates that Si dangling bond is the cause for interface states in thermally oxidised samples.

2.3 Interface Investigation

2.3.1 Experimental Techniques

Various experimental techniques have been developed for interface investigation of MOS structures [14, 15]. High frequency method of Terman [42] is useful only if interface density is large, but uncertainty about the

magnitude of the semi-conductor space charge capacitance makes this method unreliable. The low frequency capacitance method suggested by Berglund [43] gives more reliable interface state profile compared to high frequency method. The quasi-static method proposed by Kuhn 44 combines measurement of low and high frequency capacitance. But the leakage current in thin oxides being large gives rise to problems. The a.c. conductance method of Nicollian and Goetzberger [9] is the only one which gives an accurate determination of interface state density and their capture cross-section. Other recent methods like transient capacitance measurements, or deep level transient spectroscopy (DLTS) [45, 46] can be used for studying the interaction between the interface states and the minority carrier band. The a.c. conductance technique has been extended to the case of admittance measurements in a uniform background of optical illumination [11, 12]. The low frequency capacitance method also can be used with illumination [47] and the difficulties encountered in that can be overcome by using admittance method alongwith low frequency capacitance method. Above mentioned techniques though useful for thick (> 100 Å) SiO_2 interface in an MOS structure, need to be modified as outlined by Kar and Dahlke [10] for 20-40 Å thick SiO_2 interfacial. Due to the thin interfacial layer, effect of tunneling into interface states has to be considered. This has been discussed in forthcoming paragraphs of this chapter. In

the present investigation, we have employed this technique for analysis of data.

2.3.2 Low Frequency Capacitance Method

Consider the energy leveldiagram (Figure 2.2) of an MOS capacitor under a bias voltage V. In case of dark there is only the majority carrier Fermi level. When a small a.c. signal is applied, the Fermi level behaves as time varying function causing charging and discharging of interface states with a finite time constant . This may be represented by a R-C network, whose elements are given by [9]:

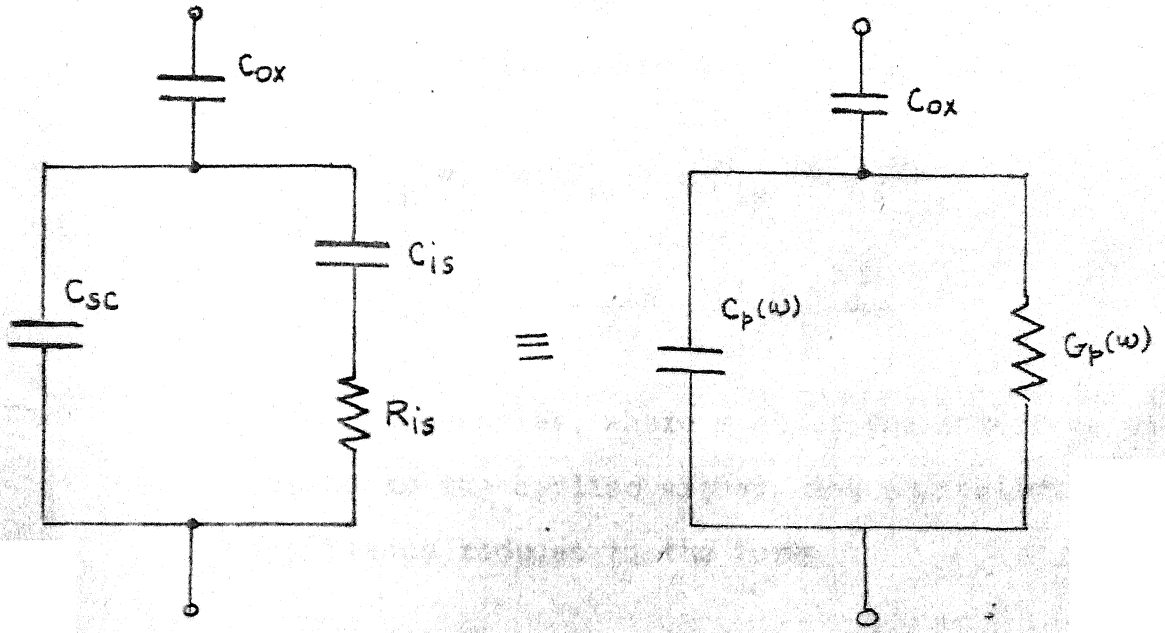
$$(a) \quad C_s = \frac{q^2 N_{ss} f_o(1 - f_o)}{kT}$$

$$(b) \quad R_s = \frac{C_s}{\tau}$$

$$(c) \quad \tau = f_o / C_p \cdot p_{so} \qquad 2.1$$

$$(d) \quad f_o = 1 + \exp(u - u_s)^{-1}$$

where f_o is the Fermi function established by the bias, u_s the normalized surface potential, p_{so} the hole density at the interface and C_p the hole capture probability of the interface state. The equivalent circuit of the MOS structure is then represented as shown in Figure 2.3. The equivalent parallel capacitance and conductance are given by [9]:



G. 2.3 EQUIVALENT CIRCUIT OF A MOS CAPACITOR WITH A SINGLE LEVEL STATE AT THE Si/SiO_2 INTERFACE

C_{sc} : SPACE CHARGE CAPACITANCE IN THE SILICON

C_{ox} : OXIDE CAPACITANCE

C_{is} : CAPACITANCE DUE TO INTERFACE STATES

$C_p(w)$: EQUIVALENT PARALLEL CAPACITANCE

R_{is} : INTERFACE STATE RESISTANCE FOR MAJORITY CARRIER RECOMBINATION

$G_p(w)$: EQUIVALENT PARALLEL CONDUCTANCE

$G_p(\omega) \equiv$ EQUIVALENT PARALLEL

$$\text{(a)} \qquad C_p(w) = \frac{C_{is}}{1 + \omega^2\tau^2} + C_{sc}$$

$$\text{(b)} \qquad C_p(w) = \frac{C_{is}\,\omega^2\tau}{1 + \omega^2\tau^2} \qquad 2.2$$

Above expressions are got on the assumption of a single level interface state. For a continuum of interface states above expressions get modified as following [30]:

$$\text{(a)} \qquad C_p(w) = C_{sc} + q\,N_{is}\,\frac{\tan^{-1}\omega\tau}{\omega\tau}$$

$$\text{(b)} \qquad C_p(w) = \frac{q\,N_{is}}{2} \cdot \frac{(1 + \omega^2\tau^2)}{\tau} \qquad 2.3$$

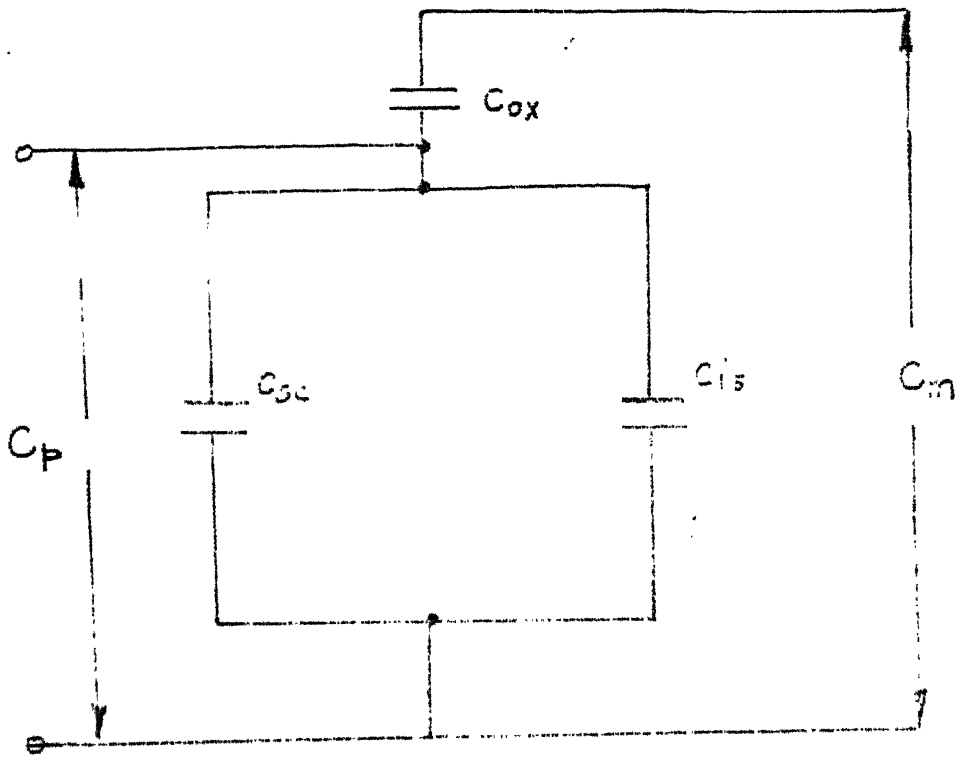
At low frequencies, where most of the interface states respond to the applied signal, the equivalent parallel capacitance reduces to the form

$$C_p(w) = C_{sc} + q\,N_{is}$$

$$= C_{sc} + C_{is}$$

and the equivalent circuit gets simplified as shown in Figure 2.4.

It is to be noted that both C_p as well as C_{sc} are functions of the interface potential. So knowing the oxide capacitance and the space charge capacitance as a function of interface potential, the interface state density is obtained as a function of interface potential and hence energy.



2.4 LOW FREQUENCY EQUIVALENT CIRCUIT FOR CIRCUIT IN FIG. 2.3. $C_p = C_{sc} + C_{is}$; C_m IS MEASURED CAPACITOR ACROSS THE DEVICE.

2.3.3 Conductance Technique

The measured admittance of an MOS capacitor consists of the oxide capacitance, space charge capacitance and the interface state admittance. The interface state admittance arises due to the charge exchange between the interface states and the silicon energy band. In case of dark, the applied signal modulates the Fermi level due to majority carriers. The minority carrier concentration cannot follow the applied signal, as they have to be thermally generated which has a longer time constant.

The admittance of the interface state depends on the distribution of the states over energy. It is observed that the interface states may occur as a single level state or as a continuum of states. The continuum of states and statistical fluctuation of the surface potential occur due to charge distribution, dopant distribution and oxide thickness distribution.

The MOS capacitor can be then represented by the equivalent circuit of Figure 2.3. The equivalent parallel conductance in the case of single level state is given by relation [9]:

$$G_p(w) = \frac{C_{is}\,\omega^2\tau}{1 + \omega^2\tau^2} \qquad \text{Single level state} \qquad 2.5$$

and

$$G_p(w) = \frac{C_{is}}{2}\,\frac{\ln(1 + \omega^2\tau^2)}{\tau} \qquad \text{Continuum of states} \qquad 2.6$$

It is seen from these equations that G_p/w goes through a maximum in both the cases and the maximum value is directly proportional to the interface state capacitance and hence interface state density:

$$\left(\frac{G_p}{w}\right)_{max.} = \frac{C_{is}}{2} = \frac{q\,N_{is}}{2} \qquad 2.7$$

$$N_{is} = \frac{2}{q}\left(\frac{G_p}{w}\right)_{max.} \qquad 2.8$$

2.3.4 Effect of Tunneling in Thin (t_{ox} 40 Å) Interfacial MOS

Above discussions are valid for thick SiO_2 interfacial typically greater than 100 Å, where no direct current is detected to flow across the junction. However, for the oxide thickness <40 Å, effect of tunneling has to be considered.

(i) In MOS structures with thin oxide films (<10 Å) the interface is in equilibrium with the metal. Schottky barrier characteristic of direct current is observed but formation of inversion layer is not possible. The device admittance does not exhibit appreciable frequency dispersion, information on the state distribution is hardly available.

(ii) In MOS structures with oxide film 20 Å $\leq t_{ox} \leq$ 40 Å, the interface is in equilibrium with the bulk silicon. However buildup of inversion layer in silicon is prevented by minority carrier flow as in thin (< 10 Å) oxide case. The applied bias generates voltage across

oxide and silicon. This causes charging effects of the states and together with the large oxide capacitance and absence of silicon-inversion, a strong dispersion of admittance curves is obtained. This allows to obtain information on the state distribution across the silicon bandgap.

Due to tunneling effect, the equivalent circuit for thick MOS as described in Figure 2.3 gets modified as shown in Figure 2.5. As can be seen in Figure 2.5(a), the equivalent circuit includes G_{TE}, the conductance associated with thermionic emission of current carriers over the silicon-barrier and then tunneling through the oxide barrier and j_{TS} a current source representing current density from metal through the oxide into the interface state.

Equivalent circuit, Figure 2.5(a) simplifies to Figure 2.5(b) for oxide thickness 20 $\mathring{A} \leq t_{ox} \leq 40$ $\mathring{A}$. The characteristic tunneling time constant of carriers from the state through the oxide into the metal τ_T being very large than interface recombination time constant for the majority carriers τ_R^{maj}. Tunneling current j_{TS} being small can be represented by a frequency independent conductance G_{TS}. Figure 2.5(c) is further simplification for low frequencies. In Figure 2.5(d), the frequency independent circuit elements C_{sc}, C_{is}, R_s^{maj} of Figure 2.5(b) are replaced by frequency dependent parallel capacitance and conductance $C_p(w)$, $G_p(w)$. Figure 2.5(e) shows the behaviour of circuit Figure 2.5(d) at low frequencies. The admittance of these MOS show strong frequency dispersion due to interface states.

A large d.c. conductance exists on which the conductance due to interface state recombination is superimposed. The a.c. conductance

$$G_{ac}(V_B, w) = G_m(V_B, w) - G_{d.c.}(V_B) \qquad 2.9$$

where $G_m(V_B, w)$ is measured total conductance, neglecting effect of bulk silicon resistance and back contact resistance.

Figures 2.5(f) and 2.5(g) show successive reduction of Figure 2.5(d). $G_{a.c.}(V_B, w)$ show sharply peaked characteristic similar to MOS structures with thick oxides. Thus, we see that due to tunneling, a d.c. conductance part gets added to $G_{a.c.}$, while we measure G_m. For applying arguments of Section 2.3.3, for evaluating interface state density, we have to subtract $G_{d.c.}$ from measured conductance G_m and use $G_{a.c.}$ for calculating $G_p(w)$, and subsequently N_{is}.

CHAPTER 3

SAMPLE FABRICATION, MEASUREMENT AND ANALYSIS

3.1 Sample Fabrication

The steps involved in fabricating ITO/nSi heterojunctions were as following:

(i) Chemical cleaning/etching of silicon wafers

(ii) Thermal oxidation

(iii) Deposition of ITO film

(iv) Annealing

(v) Back contact formation preceded by back surface etching.

The starting semiconductor material for the structure was wafers of nSi (100) surface orientation having 1.0 Ohm-cm resistivity, polished on one surface and lapped on the other, supplied by Monsanto, U.S.A. The chemical cleaning was carried out in class 100 clean environment by degreasing in warm trichloroethylene, warm acetone and warm methanol. After degreasing wafers were rinsed in deionised water having resistivity of 17-18 M Ohm-cm. The chemical cleaning was carried out till wafer surfaces became hydrophobic. Etching of wafers was done by hydrofloric acid, by rinsing in D.I. water, cleaning by HNO_3, rinsing in D.I. water, etching in HF and finally rinsing in D.I. water. The wafers were allowed to dry in class 100 clean environment.

The oxidation of silicon wafers was carried out in Heracus make furnace with electronic temperature control and monitoring. A precleaned, fused silicon tube with inlet and outlet teflon regulators was placed inside the furnace. The cleaning procedure adopted for the fused silica tube was more or less same as outlined for silicon wafers. However, after cleaning, traces of D.I. water were removed by methanol. The silicon wafers were kept in a precleaned silicon boat and the boat was introduced to about middle of silica tube, where temperature gradient was thought to be least. An oxide layer of about 20 Å thickness was grown at a steady temperature of 700°C in about 60 seconds under oxygen environment. The oxygen flow rate maintained was 45 LPH.

The deposition of junction forming ITO film was carried out by E-beam evaporation using Varian make, Ultra High Vacuum System type VT-112B. The features of Varian system and E-beam gun are provided in the Appendix 3-1. The evaporation material was Sn doped In_2O_3 in the chunk form in proportion 90% In_2O_3 and 10% SnO_2 by weight. The deposition parameters were:

System pressure	:	$8 - 10 \times 10^{-6}$ torr
Substrate temperature	:	300°C
Evaporation time	:	50 minutes
E-beam emission	:	60
Area of evaporation	:	Defined by 3.00 mm diameter Cu Masks.

Appendix 3.1 illustrates the deposition set up. The usual precautions in operating high vacuum systems are followed. Also the substrate temperature is monitored. The crucible with ITO material is cooled with recirculating chilled water to avoid the contamination of the evaporant material. Shields made of stainless steel are kept above the substrate heating filament to reflect heat to substrate and prevent excessive heating of pyrex bell jar.

Annealing was carried out in the furnace set up used for oxidation. Following process parameters and conditions were employed.

Sample No.	Temperature	Ambient	Flow rate LPH		Time Minutes
			N_2	H_2	
ENI 17	Not Annealed				
ENI 20	500°C	N_2/H_2	30	15	30

The back contacts were formed by Al metallization of the back surface of silicon wafers by filament (resistance) evaporation. The vacuum set up employed was same as deposition of ITO. Only in place of E-beam gun, resistance heating evaporation technique was employed. Procedure runs as following. The oxide layer formed on back surface of wafers was removed by etching in HF, rinsing in D.I. water and use of methanol to remove D.I. water traces. The wafers were loaded in vacuum chamber immediately after etching. 5 N purity Al, cleaned in warm TCE, warm acetone and warm methanol was also loaded into the tungsten

filament of evaporation set up of the varian system. At system pressure of 2×10^{-6} torr evaporation was carried out. The aim was to form ohmic contact.

3.2 Measurements

Electrical measurements were carried out at room temperature and in dark, with the samples placed in an electrically shield box. Electrical contact to the back contact was made through a copper block on which the samples were placed, while contact to the front gate was made with the help of a gold plated sharp pointed telescopic spring probe mounted on a micromanipulator.

The diode current versus applied bias, I-V characteristics were recorded under forward as well as reverse bias with the help of a Keithly 191 digital multimeter, a Keithly 610C electrometer and a finely adjustable power supply.

The device capacitance versus applied bias, C-V under reverse bias conditions was measured in the frequency range of 200 Hz to 10 KHz. The admittance measurements (C-V and G-V) for ENI 17 were carried out under forward as well as reverse bias under small a.c. signal, frequency range being 200 Hz to 10 KHz. For ENI-20, they could be recorded underforward bias alone for frequencies 35 Hz to 10 KHz. The impedance bridge employed for measurements was Hewlett Packard 4192 Impedance Analyser.

3.3 Data Analysis

3.3.1 Capacitance Data Analysis

Capacitance measured as a function of applied bias at low frequency (35 Hz) and high frequency (10 KHz) is analysed to get the interface state density profile based on the low frequency capacitance technique. To obtain the interface state capacitance from the measured capacitance we have to know the oxide capacitance, C_{ox}, and the space charge capacitance C_{sc}. The space charge capacitance arises due to the charging and discharging of the charge in space charge region when an a.c. signal is applied. Solution of the Poisson equation in the space charge layer gives the space charge given by the relations [14]. For nSi:

$$(a) \qquad Q_{sc} = \mp \frac{2\varepsilon_s \, kT}{q \, L_D} \cdot F\left(U_s, \frac{p_{no}}{n_{no}}\right)$$

$$(b) \qquad F\left(U_s, \frac{p_{no}}{n_{no}}\right) = \left[\left(\exp U_s - U_s - 1\right) + \frac{p_{no}}{n_{no}} \left\{\exp(-U_s) + U_s - 1\right\}\right]^{1/2} \qquad 3.1$$

$$(c) \qquad L_D = \left[2\varepsilon_s \, kT/q^2 \, n_{no}\right]^{1/2}$$

$$(d) \qquad n_{no} = N_D \; ; \qquad n_{no} \, p_{no} = n_i^2$$

$$(e) \qquad U_s = q \Psi_i / kT$$

The space charge layer capacitance is then given by the following relation [14], for nSi:

$$\frac{C_{sc}}{A} = \frac{dQ_{sc}}{d_i}$$

$$= \frac{\pm \frac{\varepsilon_s}{L_D} \left[(\exp U_s - 1) + \frac{p_{no}}{n_{no}} (\exp(- U_s) - 1) \right]}{F(U_s, \frac{p_{no}}{n_{no}})} \qquad 3.2$$

The upper sign is valid for $\Psi_i > 0$ that is band bending downwards and the lower sign for band bending upwards. Given the doping density we can calculate the space charge capacitance. The oxide capacitance, C_{ox}, is due to a plane parallel capacitance, and is hence a function of oxide thickness and permittivity alone. Assuming that the oxide thickness is uniform we can calculate the oxide capacitance

$$C_{ox} = \frac{\varepsilon_s \cdot A}{t_{ox}} \qquad 3.3$$

For sample, ENI 17, oxide thickness was estimated by oxidation parameters employed. It was estimated to be 25 Å. Though dielectric permittivity of thin thermal oxides are not known, it was assumed to be close to thick oxides (Relative permittivity 3.84).

For sample ENI 20, where saturation capacitance of the device could be extrapolated in strong accumulations, it was deduced from measured C-V curves (Figure 3.2).

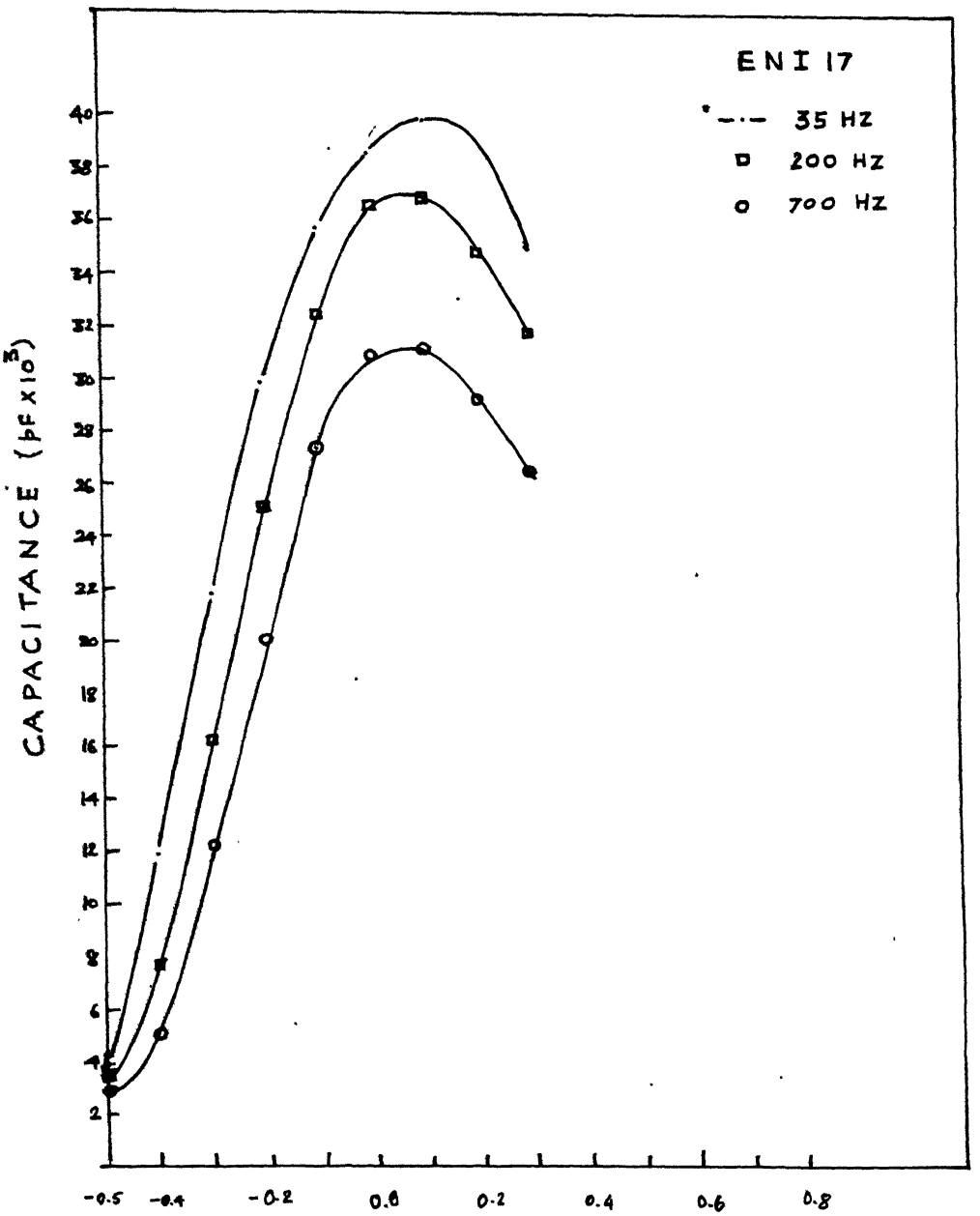

ENI 17
35 HZ
200 HZ
700 HZ
CAPACITANCE (pF x 10^3)
40
38
36
34
32
30
28
26
24
22
20
18
16
14
12
10
8
6
4
2
-0.5
-0.4
-0.2
0.0
0.2
0.4
0.6
0.8
BIAS (V)

Fig. 3.1

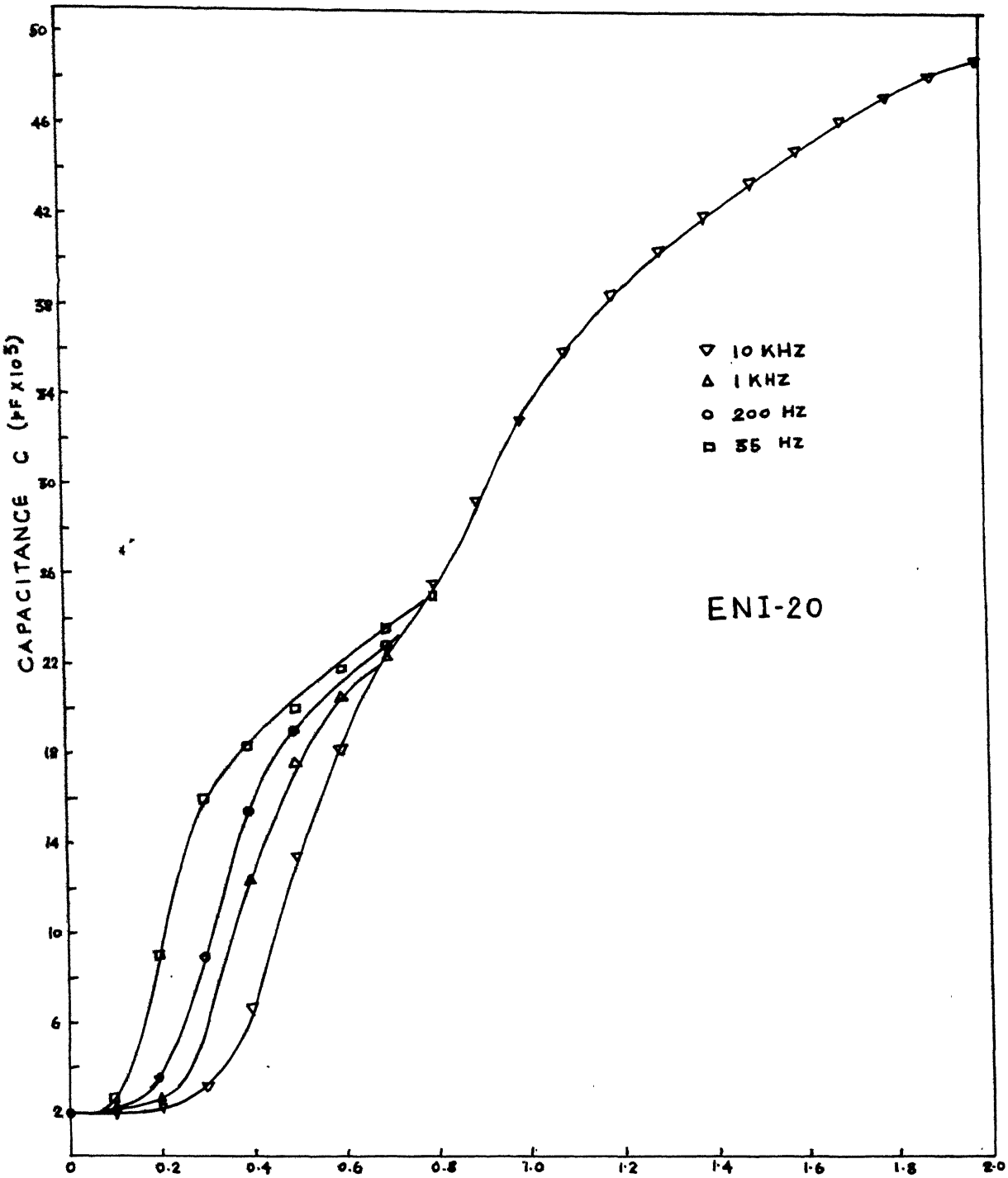

CAPACITANCE C (pF X10³)
50
46
42
38
34
30
26
22
18
14
10
6
2
0
0.2
0.4
0.6
0.8
1.0
1.2
1.4
1.6
1.8
2.0
BIAS (V)
10 KHZ
1 KHZ
200 HZ
55 HZ
ENI-20

Fig. 3.2

Evaluation of N_D and Ψ_i^o

The doping density in silicon, N_D is found from the capacitance curve measured at 10 KHz. For reverse Ψ_i in 20 Å < t_{ox} < 40 Å case is given by [10]

$$C_{sc} = [N_{Doping}\, q\, \varepsilon_s / 2(-\Psi_s - \frac{kT}{q})]^{1/2} \qquad 3.4$$

from which relation,

$$d(1/C_{sc}^2)/dV_B = [2/(N_{Doping}\, q\, \varepsilon_s)] \frac{d\Psi_i}{dv} \qquad 3.5$$

is easily obtained. Expression for $d\Psi_i/dv$ can be substituted in equation 3.5 for oxide tunneling case cf. Figure 3.2(c)

$$\frac{d\Psi_i}{dv} = 1/[1 + (C_{sc} + C_{is})/C_{ox}] \simeq 1 \qquad 3.6$$

above approximation is valid, since $C_{ox} >> C_{sc} + C_{is}$ $C_{measured}$ is fulfilled for a large oxide capacitance and a large reverse Ψ_i.

We see from equations 3.5 and 3.6,

$$N_{doping} = 2/[q\, \varepsilon_s / \frac{d(1/C^2)}{dv}] \qquad 3.7$$

In Figures 3.3 and 3.4, $1/C^2 - V$ is plotted for samples ENI 17 and ENI 20 respectively.

Thus N_{doping}, using Figures 3.3 and 3.4, is determined from the slope of $1/C^2 - V$ curves. Under forward Ψ_i, $1/C^2 - V$ is not a straight line due to influence of interface states. N_{Doping} is usually different from that in

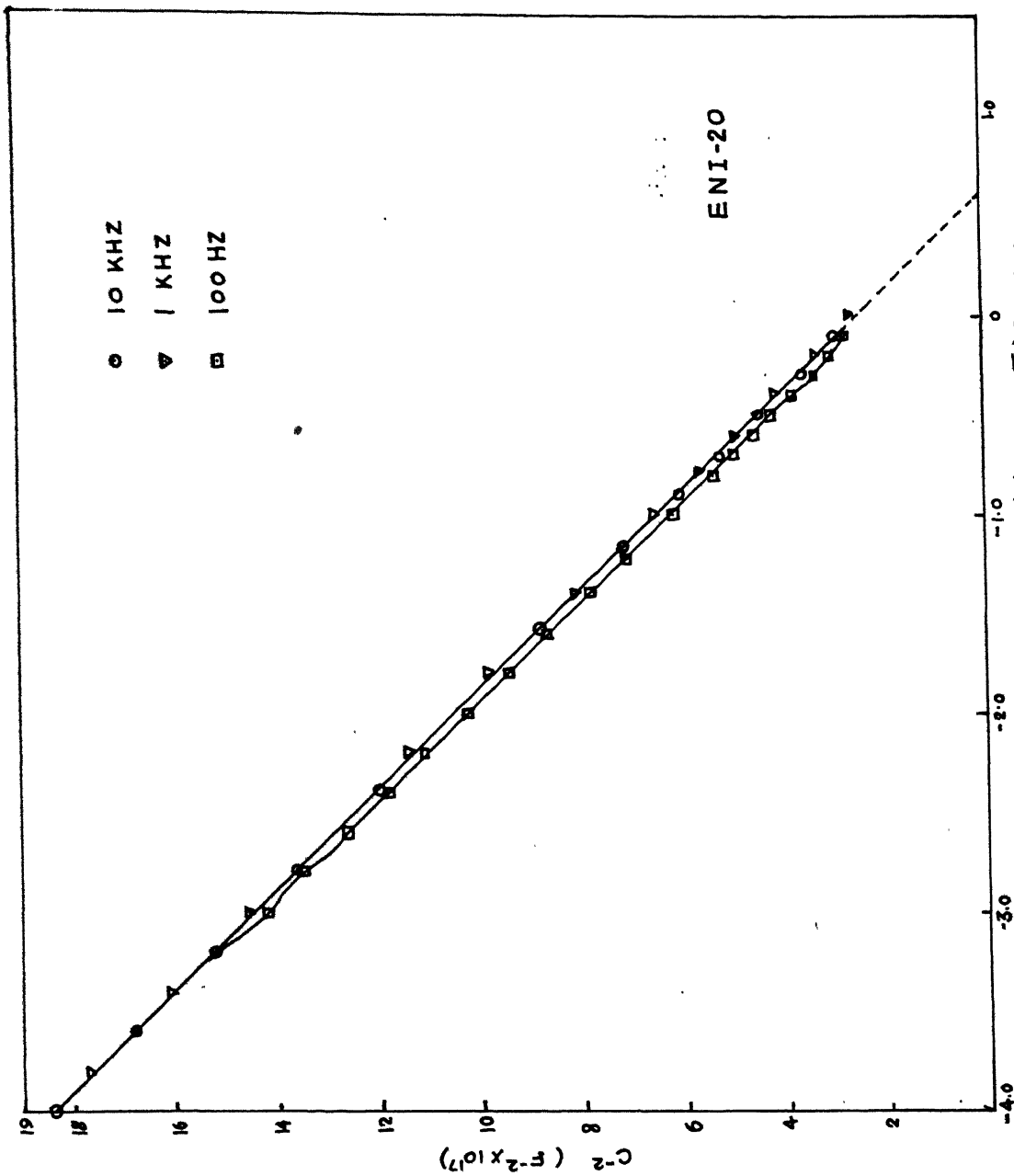

ENI-20
10 KHZ
1 KHZ
100 HZ
C⁻² (F⁻² x 10¹⁷)
BIAS (V)
19
18
16
14
12
10
8
6
4
2
1.0
0
-1.0
-2.0
-3.0
-4.0

FIG 3.4

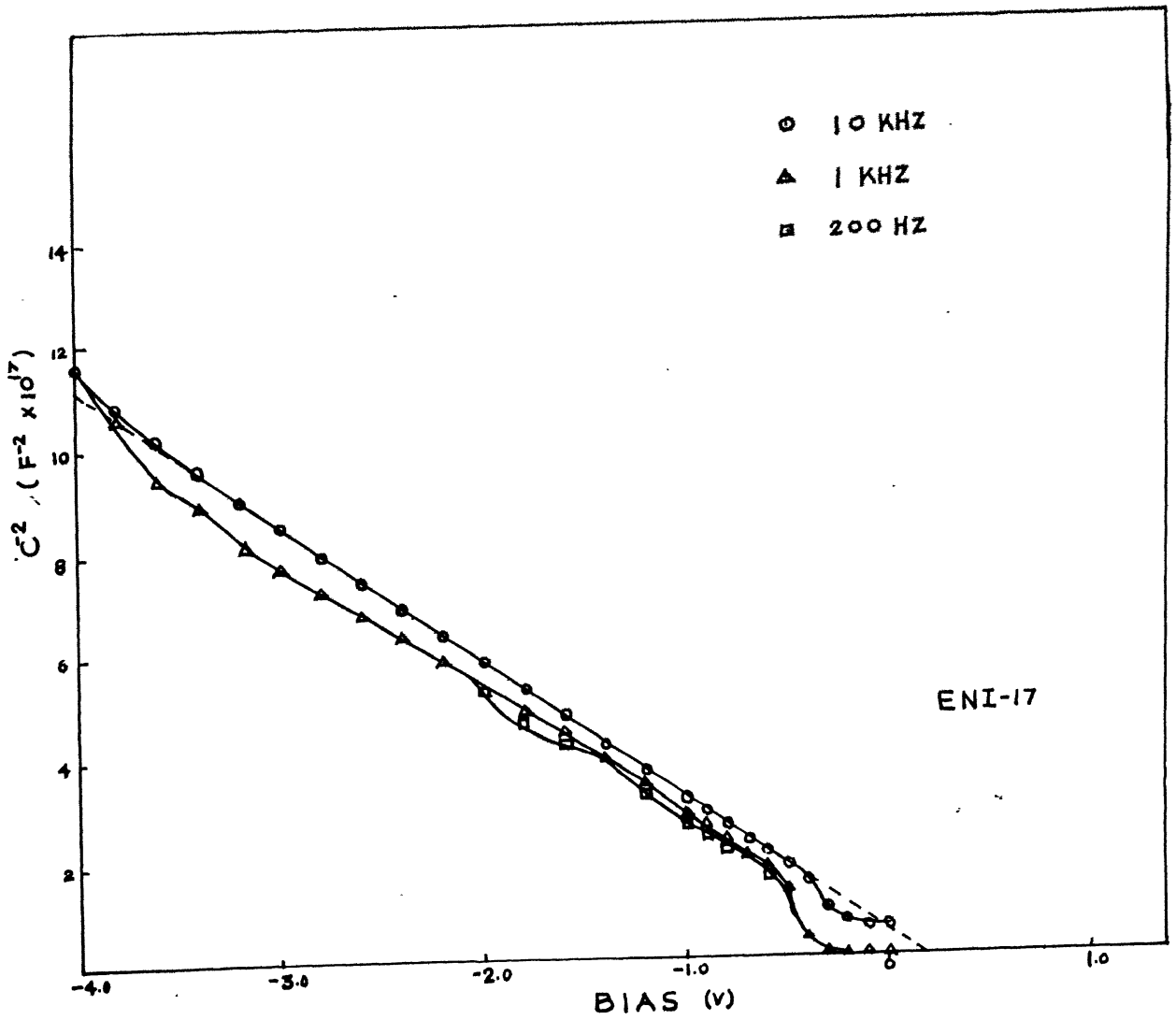

10 KHZ
1 KHZ
200 HZ
ENI-17
C^{-2} (F^{-2} x 10^{17})
14
12
10
8
6
4
2
-4.0
-3.0
-2.0
-1.0
0
1.0
BIAS (V)

FIG 3.3

the bulk because of redistribution during thermal oxidation, but this uncertainty does not affect the evaluated interface state density distribution.

By integrating equation 3.7, we obtain

$$\frac{1}{C^2} = 2(-\Psi_i^o + V - \frac{kT}{q})/(N_{Doping}\ q\ \varepsilon_s)$$

the zero bias surface potential Ψ_i^o,

$$\Psi_i^o = V_{intercept} - \frac{kT}{q} \qquad 3.8$$

where $V_{intercept}$ is bias-axis intercept of extrapolated $1/C^2 - V$ curve, cf. Figures 3.3 and 3.4.

Evaluation of $\Psi_i(V)$

The interface potential Ψ_i as a function of applied bias V is obtained by graphically integrating the measured low frequency C-V characteristics, based on relation [43],

$$\Psi_i(V_1) - \Psi_i(V_2) = \int_{V_1}^{V_2} (1 - \frac{C_{l.f.}}{C_{ox}})dv + C \qquad 3.9$$

where C is a constant, $C_{l.f.}$ is the capacitance at sufficiently low or equilibrium frequency. For sample, ENI 17, the 35 Hz curve was used, cf. Figure 3.1. Integration was carried out at estimated C_{ox} value, as explained earlier.

For sample ENI 20, the low frequency 35 Hz curve was used for integration to evaluate Ψ_i. In this case capacitance has tendency to saturate under large forward bias and hence shows accumulation.

From experimentally determined value of N_D, C_{sc} was evaluated using equation 3.2. A semilog graph of $C_{sc} - \Psi_i(V)$ was plotted as shown in Figures 3.5 and 3.6.

The measured low frequency capacitance $C_{l.f.}$ is reduced to equivalent parallel capacitance C_p, cf. Figure 2.4

$$\frac{1}{C_p^{l.f.}(V)} = \frac{1}{C^{l.f.}(V)} - \frac{1}{C_{ox}}$$

Initially, estimated value of C_{ox} is used to evaluate $C_p^{l.f.}$. If the estimated C_{ox} is correct the experimental ln $C_p^{l.f.}$ versus Ψ_i and theoretical ln C_{sc} versus Ψ_i plots should have same slope under strong accumulation, since under strong accumulation parallel capacitance is mainly due to space charge capacitance. By a few iterations, an accurate value of C_{ox} is determined. For sample ENI 17, where low frequency capacitance does not saturate under strong accumulation, C_{ox} was determined by oxidation parameter as described earlier.

For sample, ENI 20, where low frequency measured capacitance has tendency to saturate, the accurate value of C_{ox} was determined by matching slope of ln $C_p^{l.f.}$ versus Ψ_i and ln C_{sc} versus Ψ_i plots. After C_{ox} was accurately determined, the linear part of experimental ln $C_p^{l.f.}$ versus Ψ_i curve is fitted with calculated ln C_{sc} versus Ψ_i curve to get constant C.

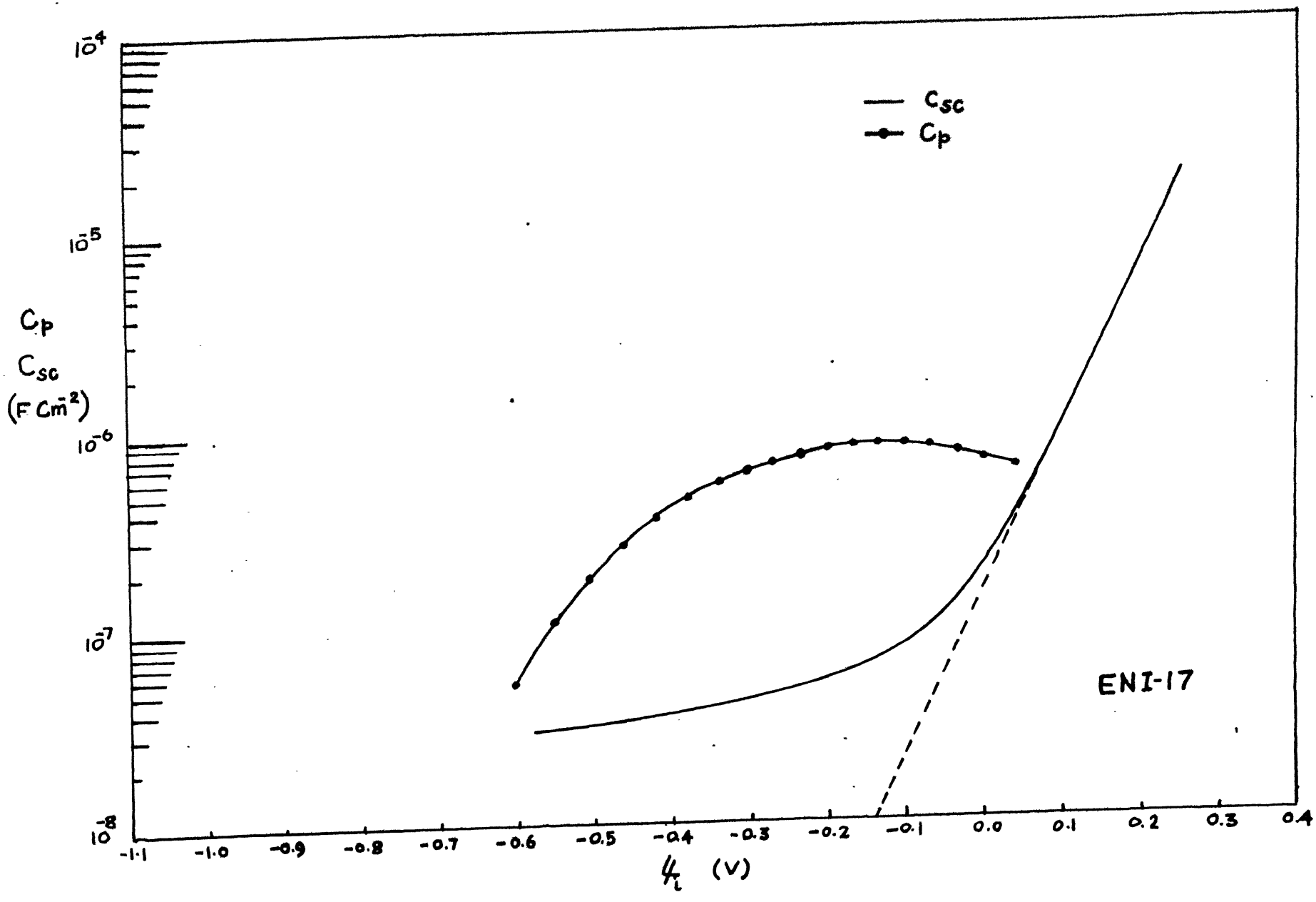

C_{sc}
C_p
10^{-4}
10^{-5}
10^{-6}
10^{-7}
10^{-8}
C_p
C_{sc}
$(F\,Cm^{-2})$
ENI-17
-1.1
-1.0
-0.9
-0.8
-0.7
-0.6
-0.5
-0.4
-0.3
-0.2
-0.1
0.0
0.1
0.2
0.3
0.4
ψ_i (V)

Fig. 3.5

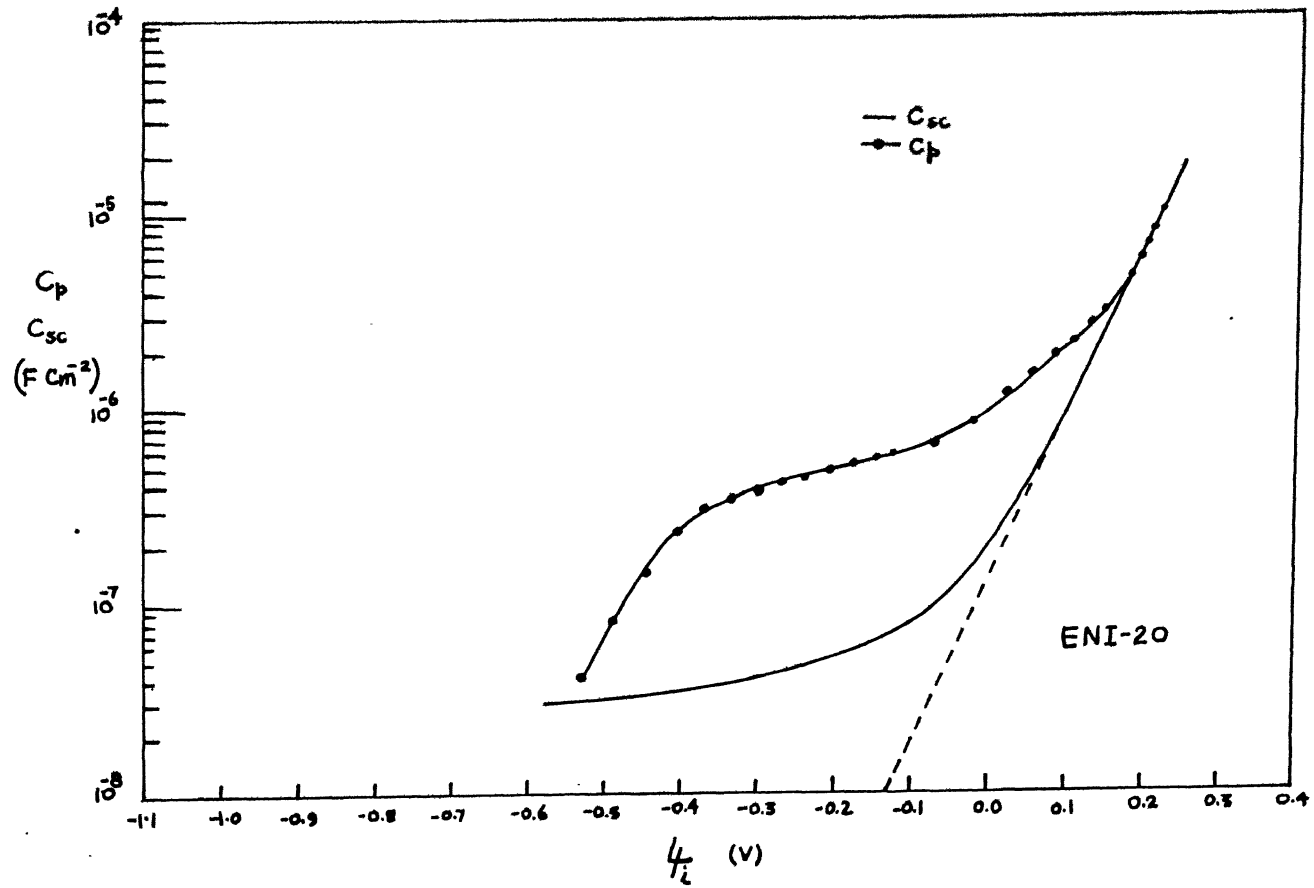

C_{sc}
C_p
ENI-20
C_p
C_{sc}
$(F\,cm^{-2})$
10^{-4}
10^{-5}
10^{-6}
10^{-7}
10^{-8}
-1.1
-1.0
-0.9
-0.8
-0.7
-0.6
-0.5
-0.4
-0.3
-0.2
-0.1
0.0
0.1
0.2
0.3
0.4
ϕ_i (V)

Fig. 3.6

With determination of C_{ox} and constant C, integration as per equation 3.9 is carried out and a plot of Ψ_i versus V as shown in Figures 3.7 and 3.8 is obtained for samples ENI 17 and ENI 20 respectively. Also using thus determined C_{ox}, $C_p^{l.f.}(V)$ is calculated and a plot of $\ln C_p^{l.f.}$ versus Ψ_i is obtained as shown in Figures 3.5 and 3.6 for sample ENI 17 and ENI 20 respectively.

Evaluation of Interface Density N_{is} and its Energy Location

The interface capacitance according to Figure 2.4,

$$C_{is} = C_p - C_{sc} \qquad 3.10$$

is obtained by subtracting the calculated space charge capacitance C_{sc} from measured parallel capacitance as evaluated earlier at low frequency. The interface state density N_{is} as a function of surface potential Ψ_i is obtained as:

$$N_{is} = \frac{C_{is}}{q} \quad (cm^{-2}\ v^{-1}) \qquad 3.11$$

The energy location corresponding to an interface state are given by, for nSi

$$E - E_v = E_g - q\,(\phi_n + \Psi_i) \qquad 3.12$$

A plot of N_{is} $-(E - E_v)$ is shown in Figures 3.9 and 3.10 for samples ENI 17 and ENI 20 respectively.

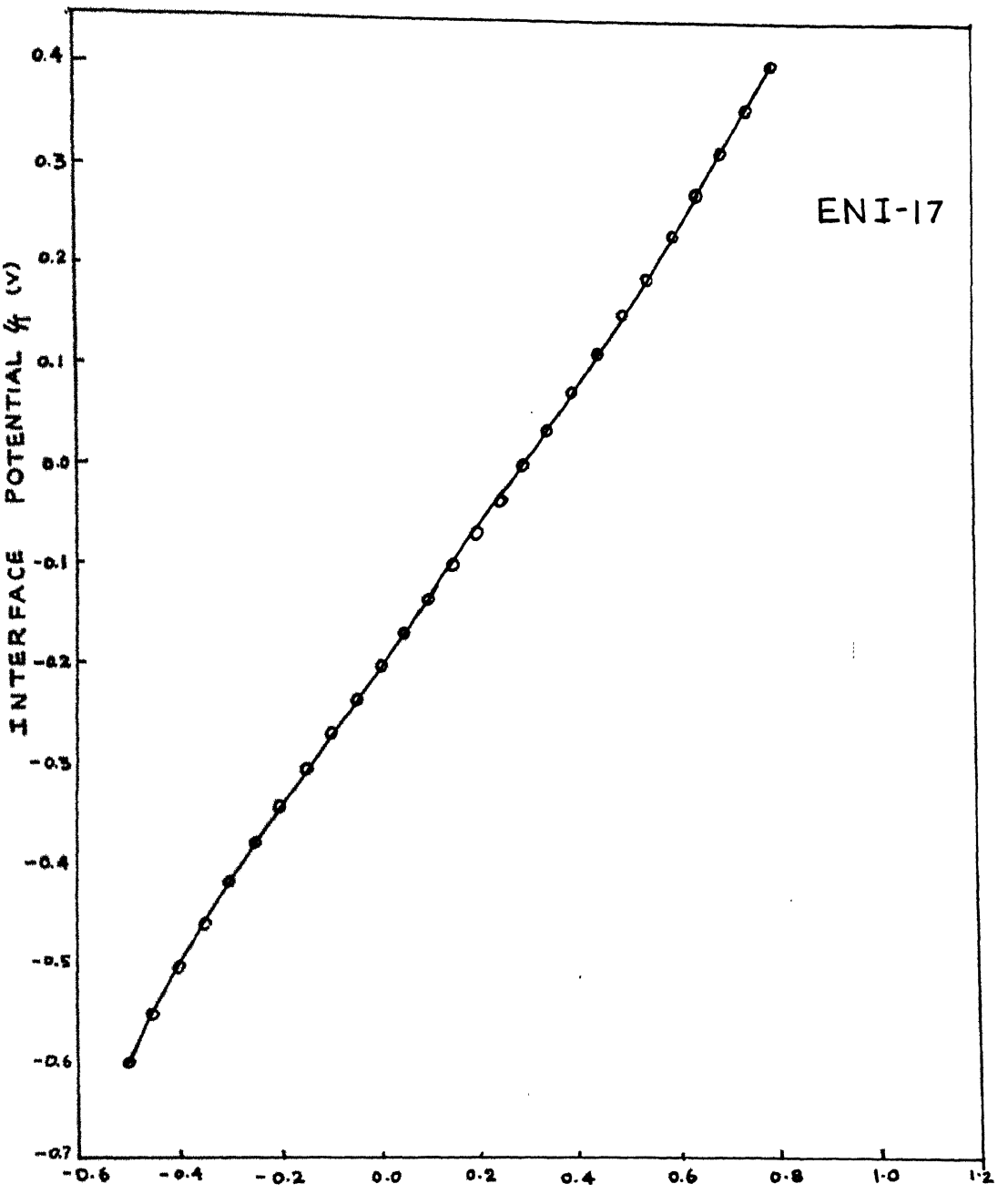

ENI-17
INTERFACE POTENTIAL ψ_s (V)
0.4
0.3
0.2
0.1
0.0
-0.1
-0.2
-0.3
-0.4
-0.5
-0.6
-0.7
-0.6
-0.4
-0.2
0.0
0.2
0.4
0.6
0.8
1.0
1.2
BIAS (V)

Fig. 3.7

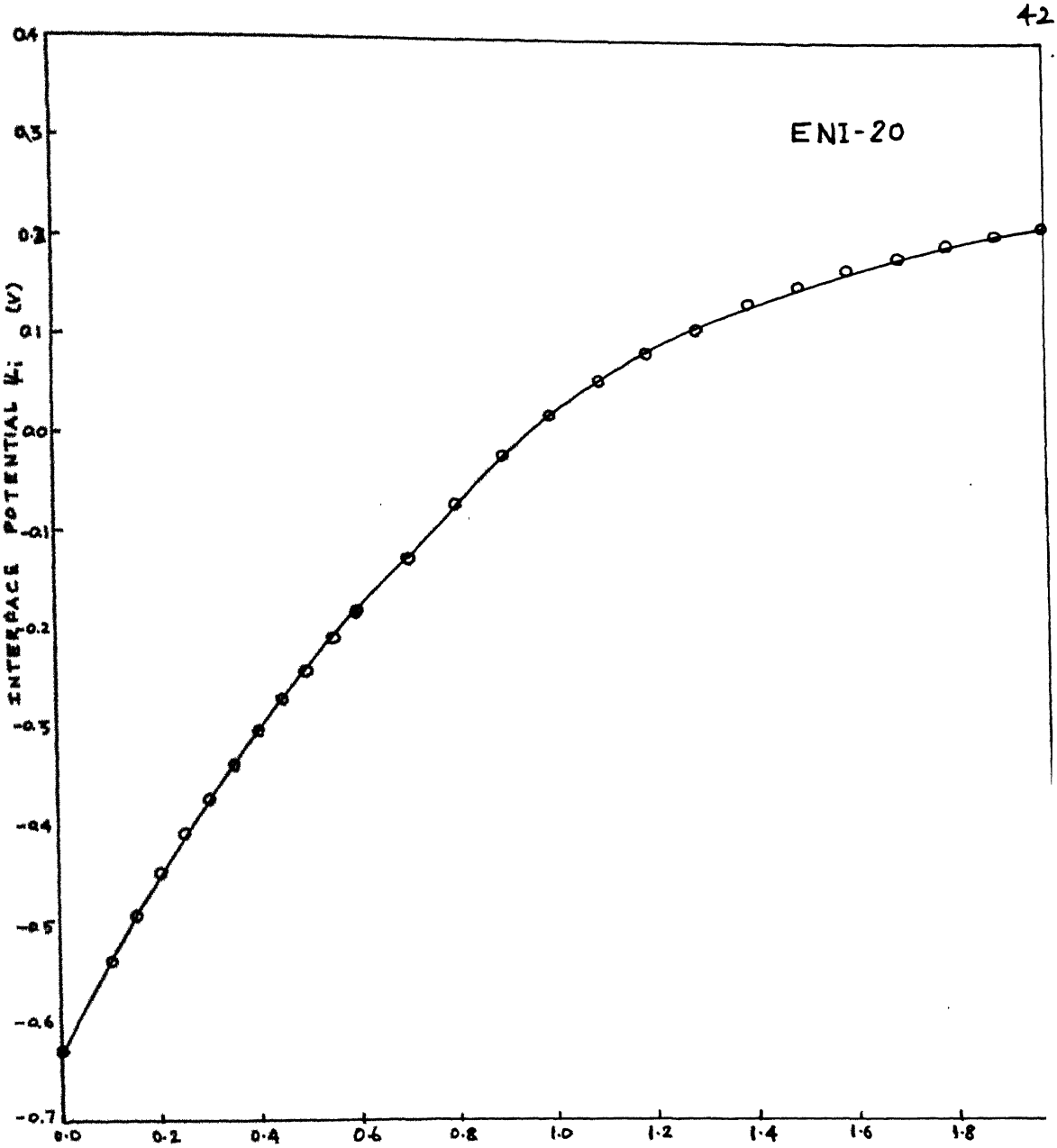
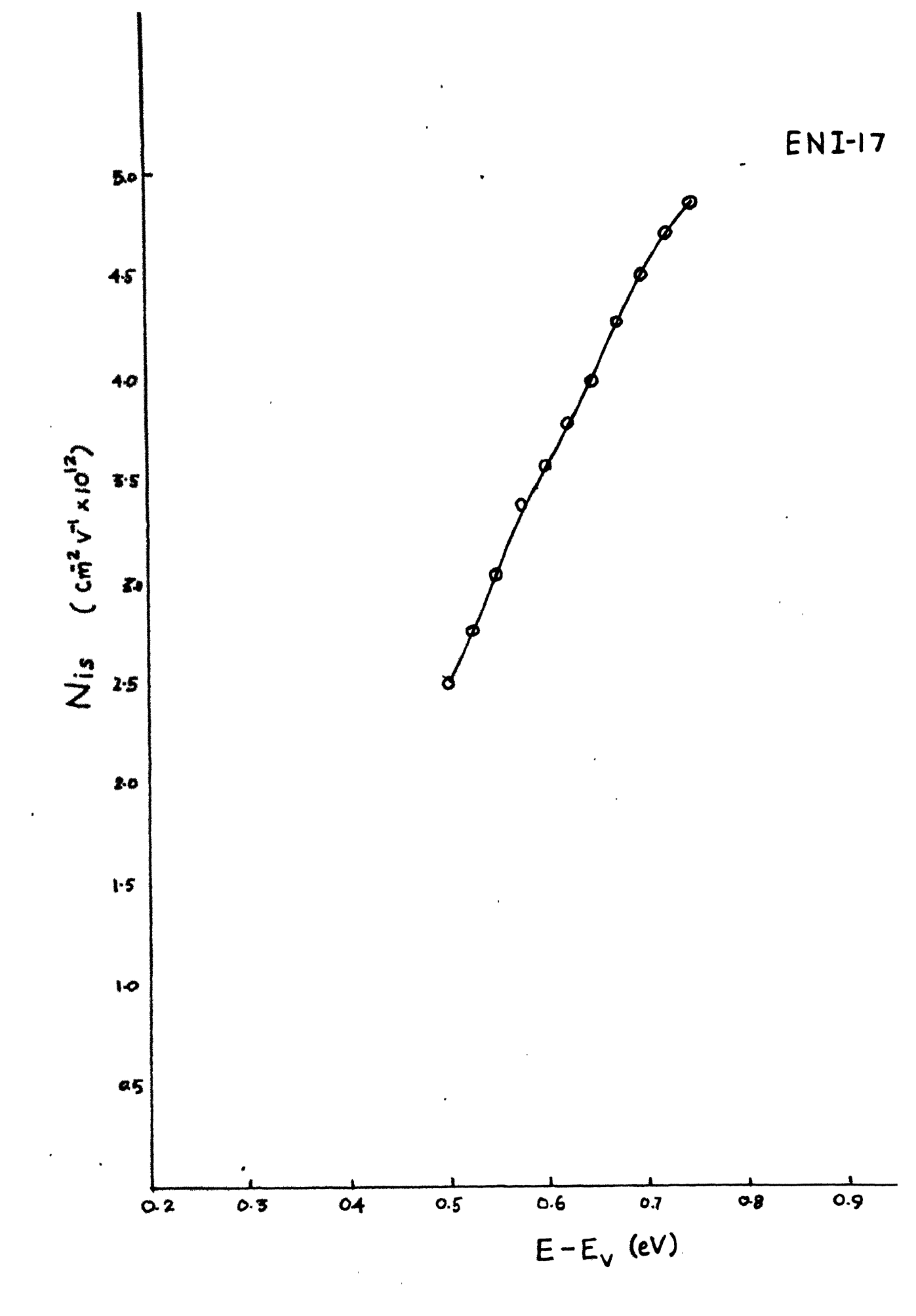
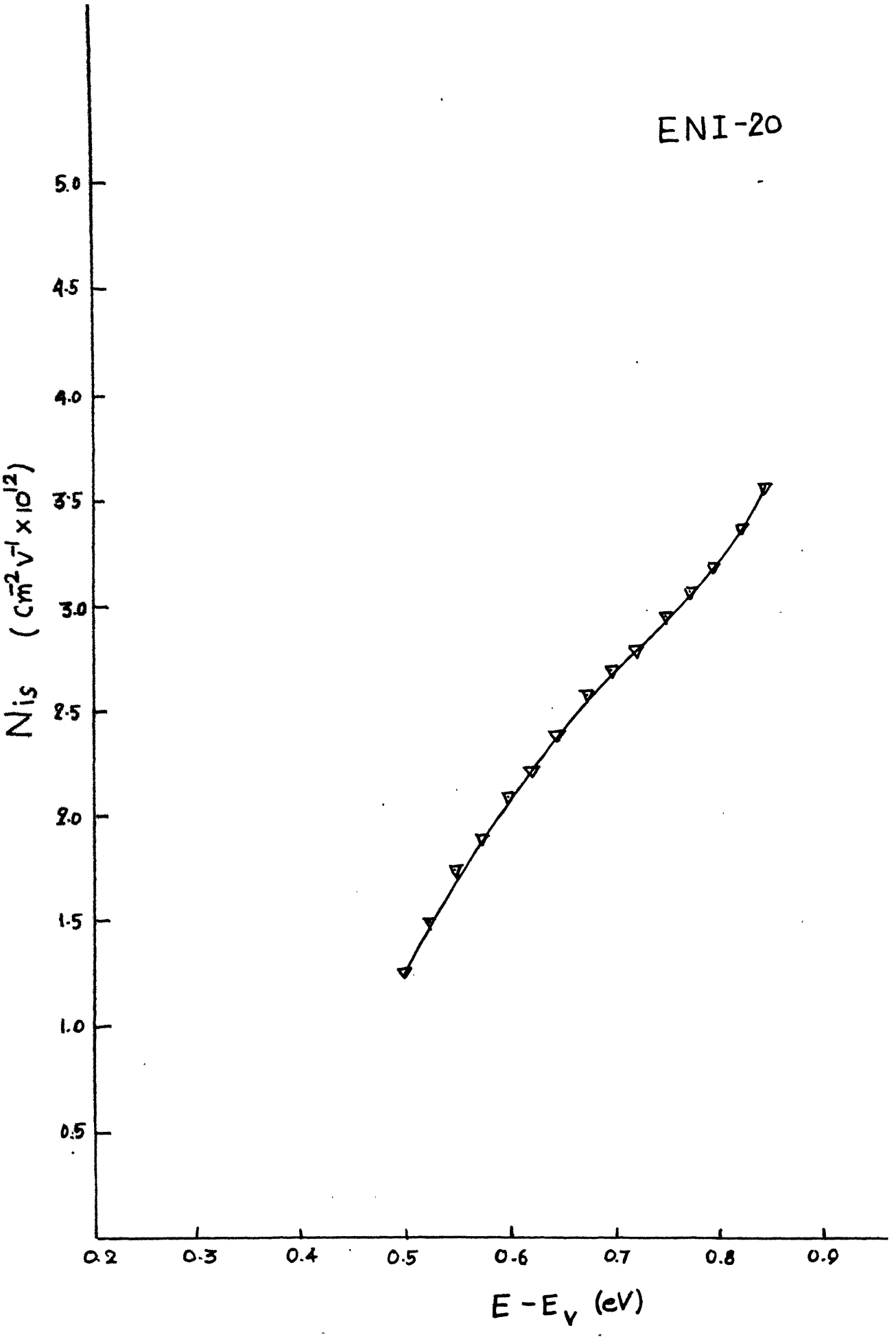

ENI-20
INTERFACE POTENTIAL ψ_i (V)
0.4
0.3
0.2
0.1
0.0
-0.1
-0.2
-0.3
-0.4
-0.5
-0.6
-0.7
0.0
0.2
0.4
0.6
0.8
1.0
1.2
1.4
1.6
1.8
BIAS (V)

Fig. 3.8


ENI-17
5.0
4.5
4.0
3.5
3.0
2.5
2.0
1.5
1.0
0.5
N_{is} ($cm^{-2}V^{-1} \times 10^{12}$)
0.2
0.3
0.4
0.5
0.6
0.7
0.8
0.9
$E - E_V$ (eV)


ENI-20
5.0
4.5
4.0
3.5
3.0
2.5
2.0
1.5
1.0
0.5
N_{is} ($cm^{-2}V^{-1} \times 10^{12}$)
0.2
0.3
0.4
0.5
0.6
0.7
0.8
0.9
$E - E_V$ (eV)

3.3.2 Conductance Analysis

The measured conductance G_m versus V characteristics at various frequencies are plotted in Figures 3.13 and 3.14, for the sample ENI 17 and ENI 20 respectively.

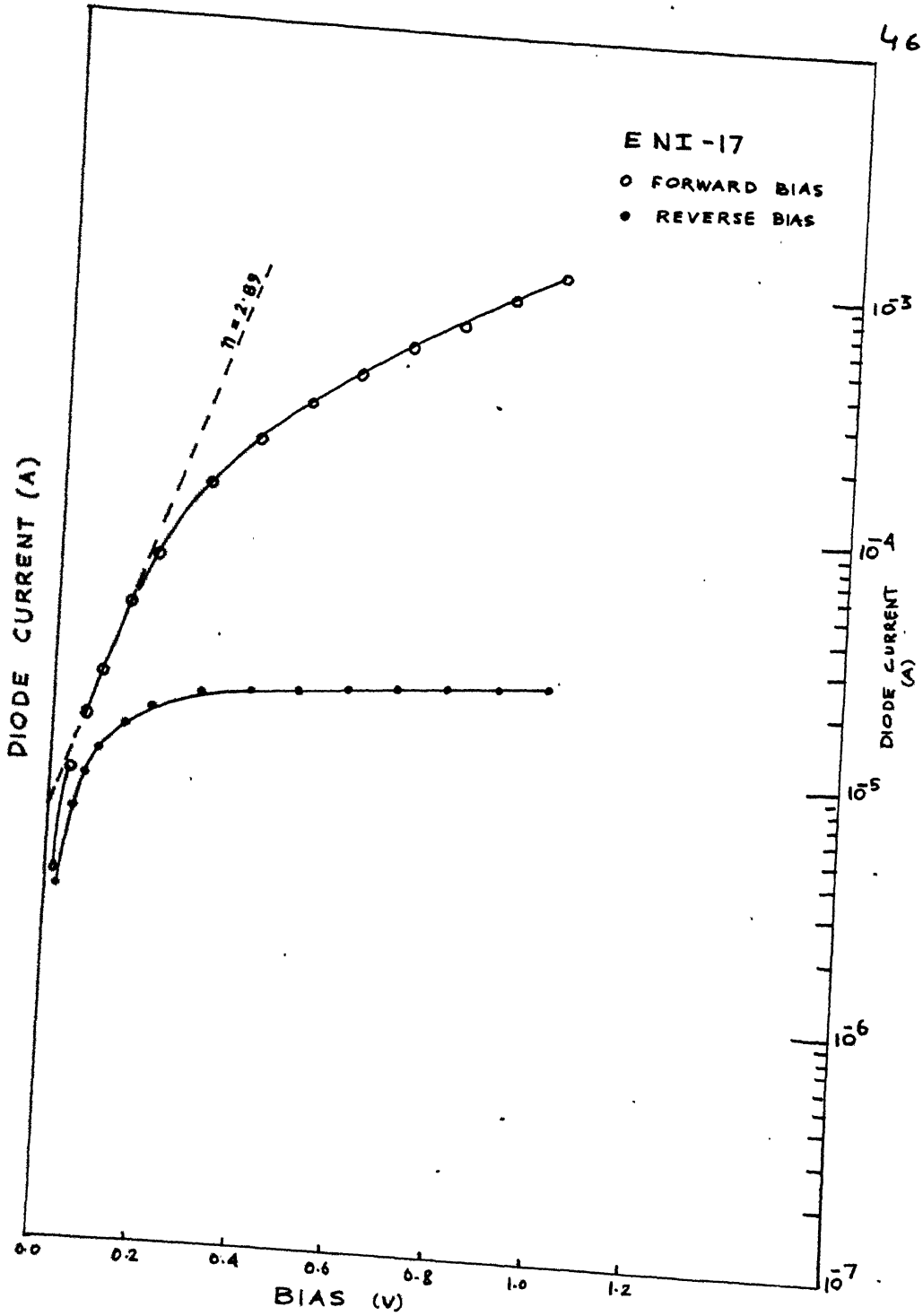
As outlined, in conductance technique in Section 2.3.3, the interface state density distribution N_{is} could be determined by using the maxima of (G_p/w) of the $G_p(V,w)/w$ curves. Also, G_m, the measured conductance contains a frequency dependent conductance $G_{a.c.}$, as well as direct current conductance $G_{d.c.}$, arising due to tunneling effect. Thus, to evaluate $G_{a.c.}$, $G_{d.c.}$ is to be obtained. $G_{d.c.}$ is obtained by graphical differentiation of current-voltage characteristics of devices. Current-voltage characteristic of the devices are as shown in Figures 3.11 and 3.12 for the samples ENI 17 and ENI 20 respectively. To evaluate $G_{a.c.}$, use of equation 2.9 is made

$$G_{a.c.} = G_m - G_{d.c.}$$

Evaluation of $G_{a.c.}$ is done for different frequencies, and plots of $G_{a.c.}$ versus V are obtained, as shown in Figures 3.15 and 3.16 for the samples ENI 17 and ENI 20 respectively.

The equivalent parallel conductance G_p, in terms of measured conductance is given by following relation [9]

$$\frac{G_p}{w} = \frac{w C_{ox}^2 G_m}{G^2 + w^2(C_{ox} - C_{})^2} \qquad 3.1$$


ENI-17
FORWARD BIAS
REVERSE BIAS
η = 2.89
DIODE CURRENT (A)
10⁻³
10⁻⁴
10⁻⁵
10⁻⁶
10⁻⁷
DIODE CURRENT (A)
0.0
0.2
0.4
0.6
0.8
1.0
1.2
BIAS (V)

Fig·3·11

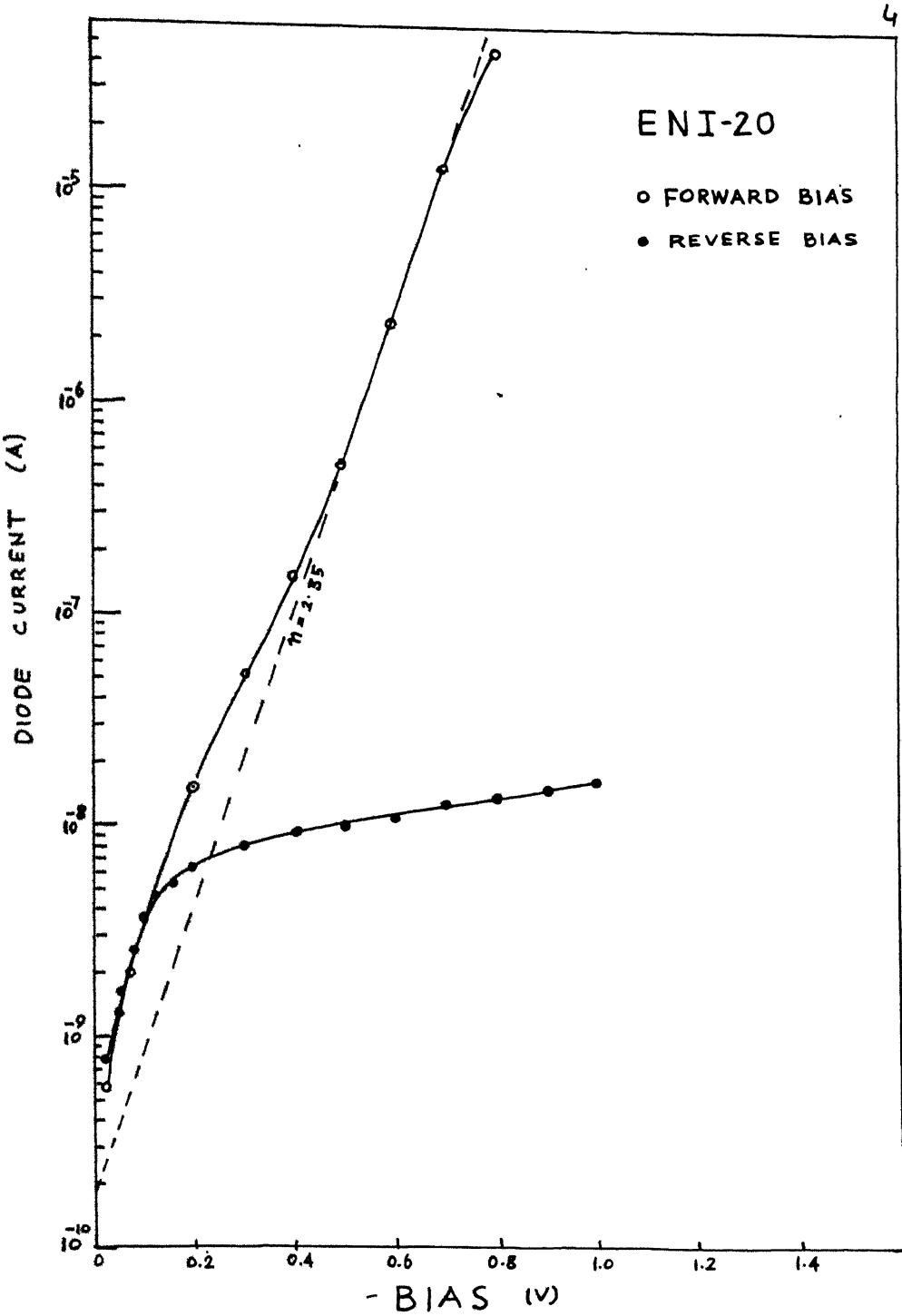

ENI-20
o FORWARD BIAS
• REVERSE BIAS
DIODE CURRENT (A)
10^{-5}
10^{-6}
10^{-7}
10^{-8}
10^{-9}
10^{-10}
$\eta = 2.35$
0
0.2
0.4
0.6
0.8
1.0
1.2
1.4
- BIAS (V)

Fig 3.12

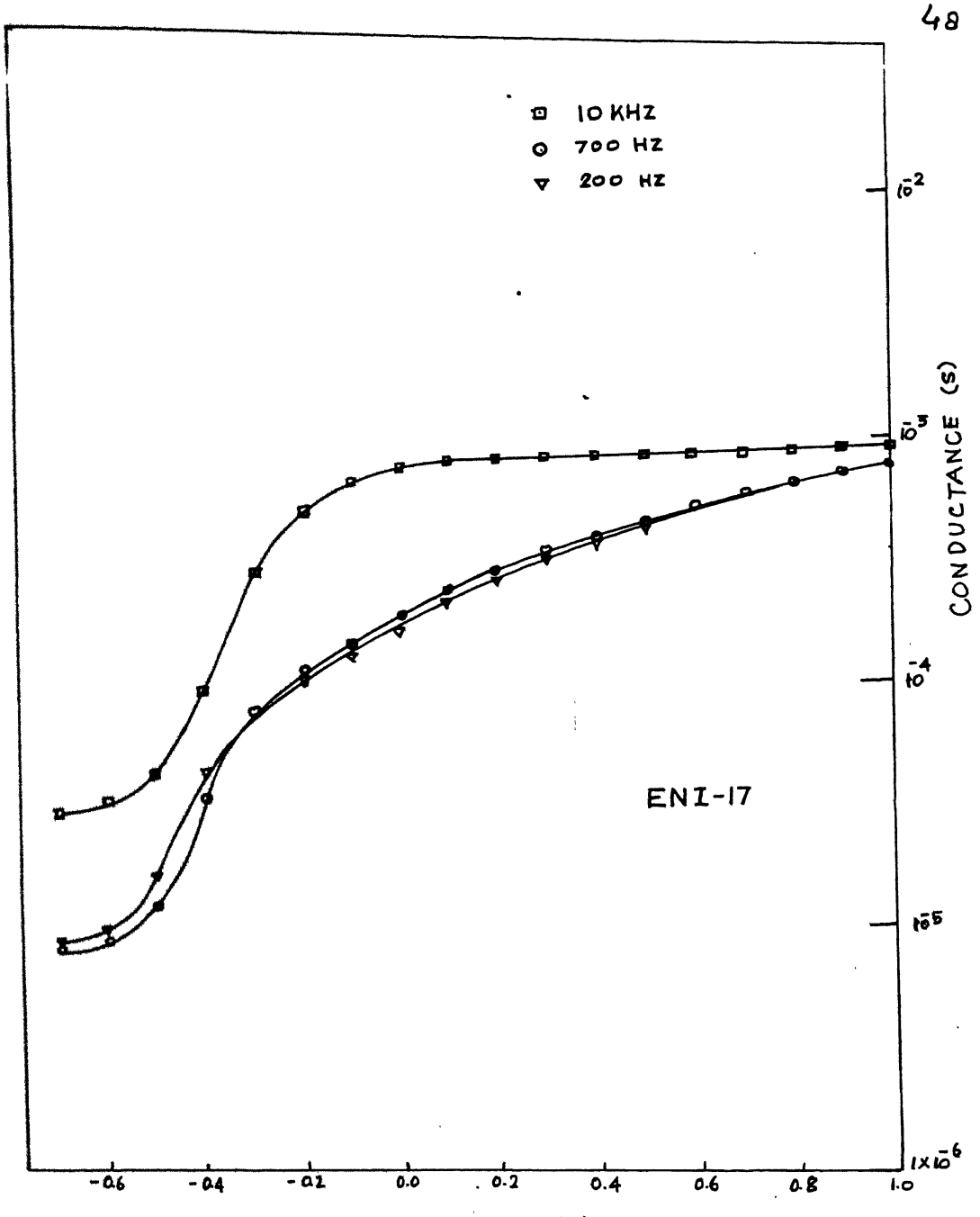

10 KHZ
700 HZ
200 HZ
ENI-17
10^{-2}
10^{-3}
10^{-4}
10^{-5}
1×10^{-6}
CONDUCTANCE (S)
-0.6
-0.4
-0.2
0.0
0.2
0.4
0.6
0.8
1.0
BIAS (V)

Fig. 3.13

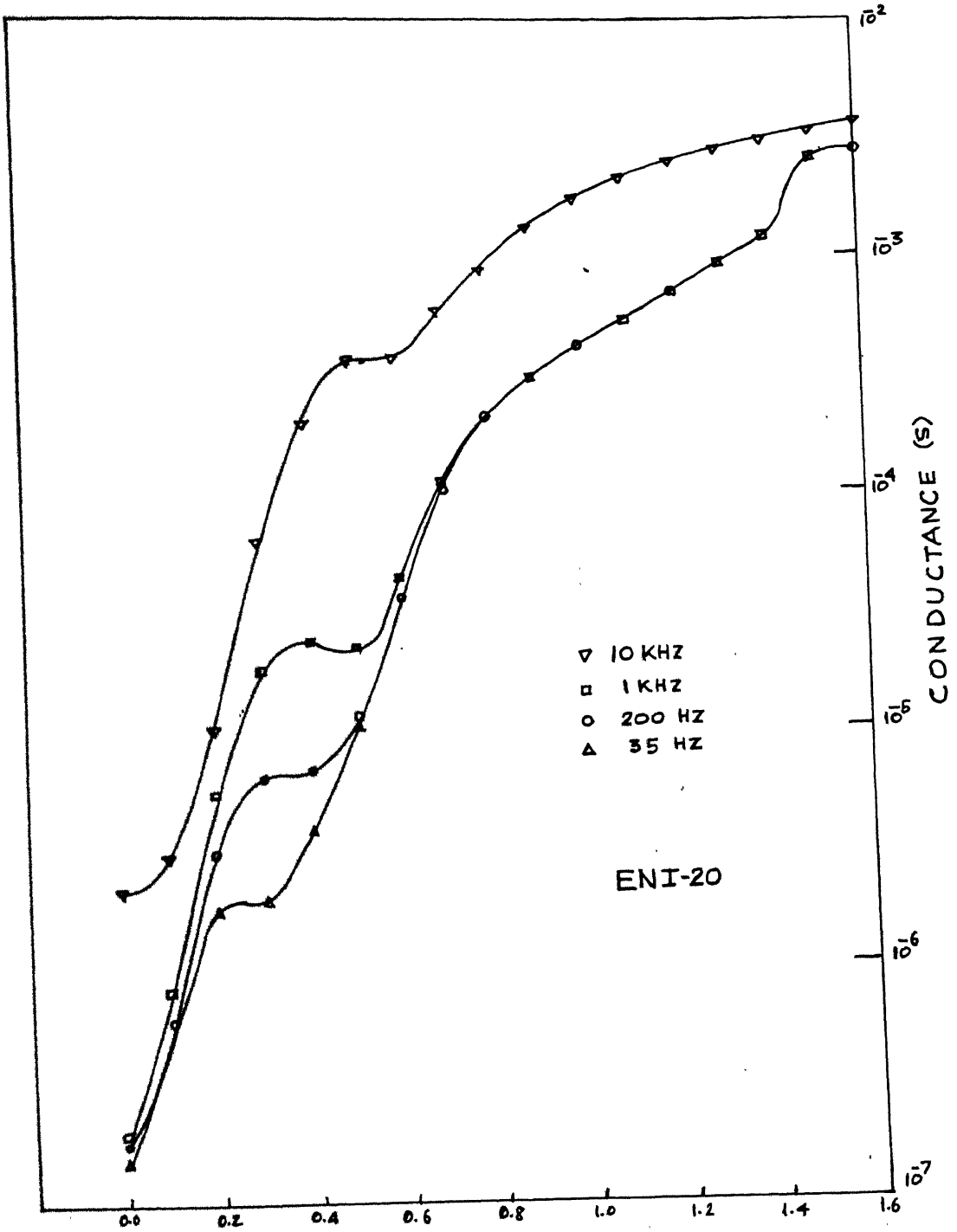

10^{-2}
10^{-3}
10^{-4}
10^{-5}
10^{-6}
10^{-7}
CONDUCTANCE (S)
▽ 10 KHZ
□ 1 KHZ
○ 200 HZ
△ 35 HZ
ENI-20
0.0
0.2
0.4
0.6
0.8
1.0
1.2
1.4
1.6
BIAS (V)

Fig. 3.14

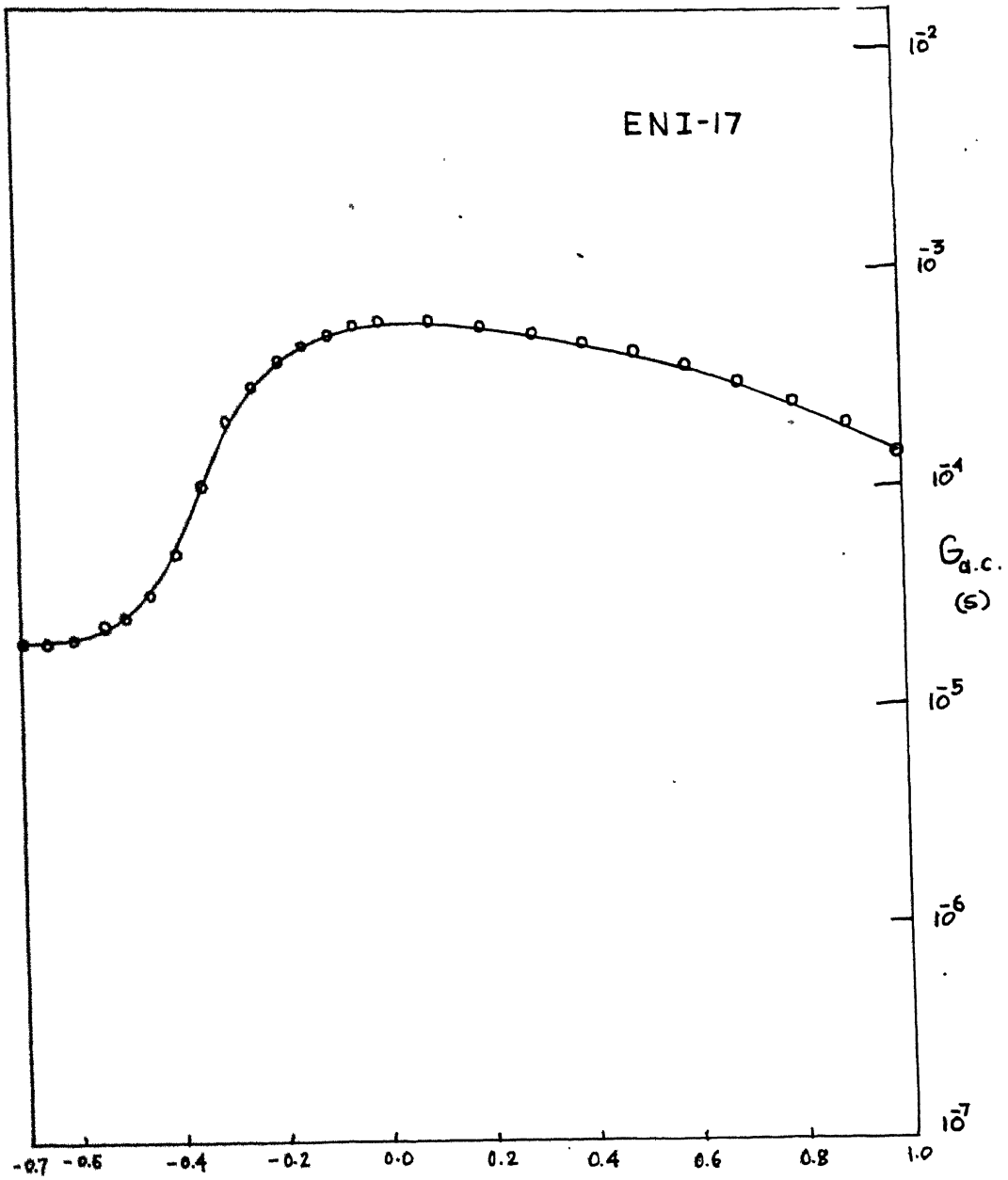

ENI-17
10^{-2}
10^{-3}
10^{-4}
10^{-5}
10^{-6}
10^{-7}
$G_{a.c.}$ (S)
-0.7 -0.6 -0.4 -0.2 0.0 0.2 0.4 0.6 0.8 1.0
BIAS (V)

Fig. 3.15

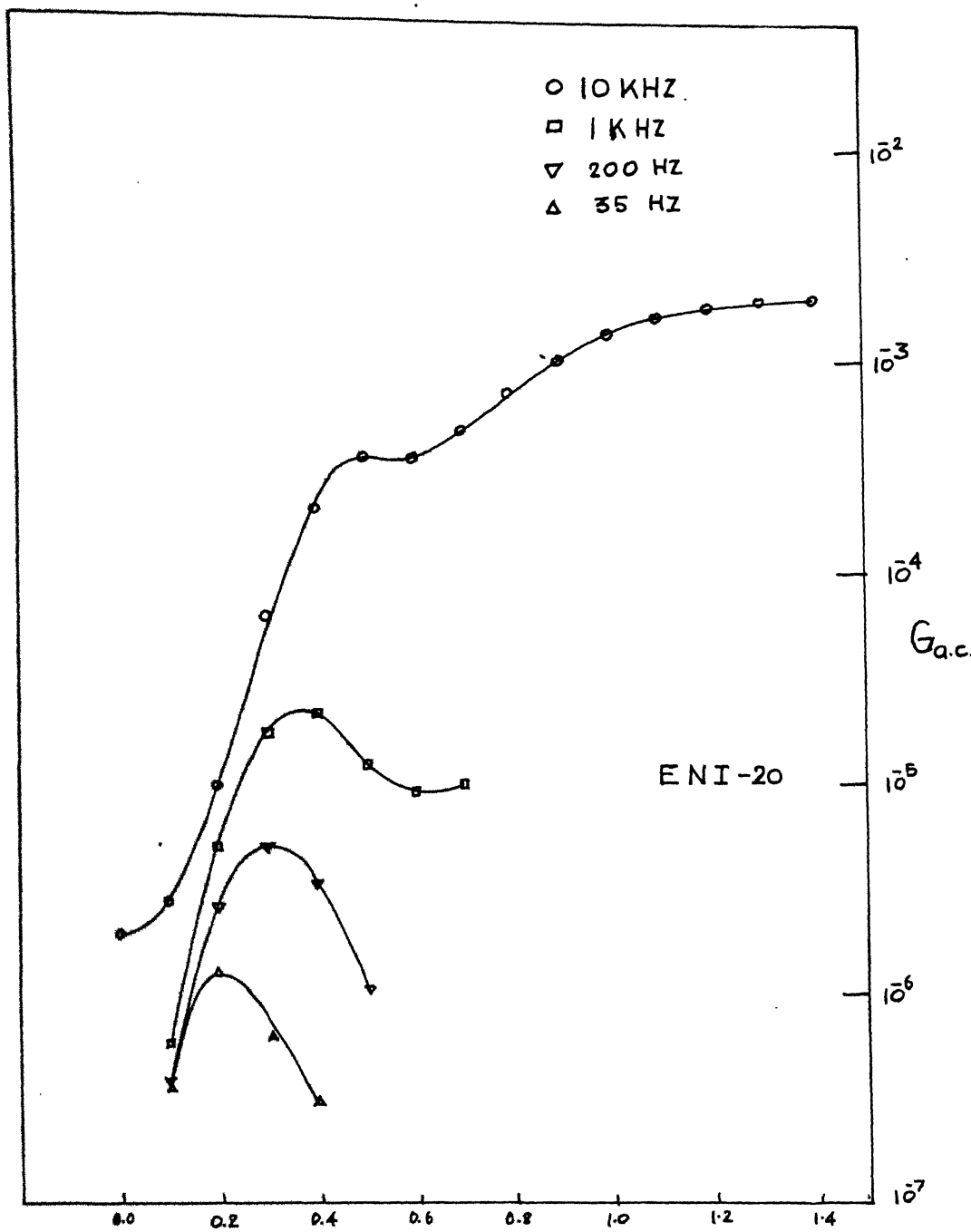


Fig. 3.16

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In our case, calculated $G_{a.c.}$ is used in place of G_m, in the above equation for the arguments provided in Section 2.3.4 and the equation 3.13 may be written as

$$\frac{G_p}{w} = \frac{w\, C_{ox}^2\, G_{a.c.}}{G_{a.c.}^2 + w^2(C_{ox} - C_m)^2}$$

G_p/w is calculated at different bias voltage, for various frequencies. Figures 3.17 and 3.18 show plots for G_p/w versus V for ENI 17 and ENI 20 respectively.

The various peaks of G_p/w correspond to the interface states. Identification of the source of conductance peak is done by comparing the half width of the G_p/w versus f with theoretical curves as obtained by Nicollian and Goetzberger [9], the most appropriate model for distribution of interface states is decided.

For a single level state, G_p/w plotted as bias or frequency goes through a peak at $w\tau = 1$, and G_p/w is given as [9]

$$\left(\frac{G_p}{w}\right)_{max.} = \frac{C_{is}}{2} = \frac{q \cdot A \cdot N_{is}}{2}$$

The interface state density and time constant are given as

$$\text{(a)} \qquad N_{is} = \frac{2(G_p/w)_{max.}}{q \cdot A} \qquad 3.14$$

$$\text{(b)} \qquad \tau = 1/w$$

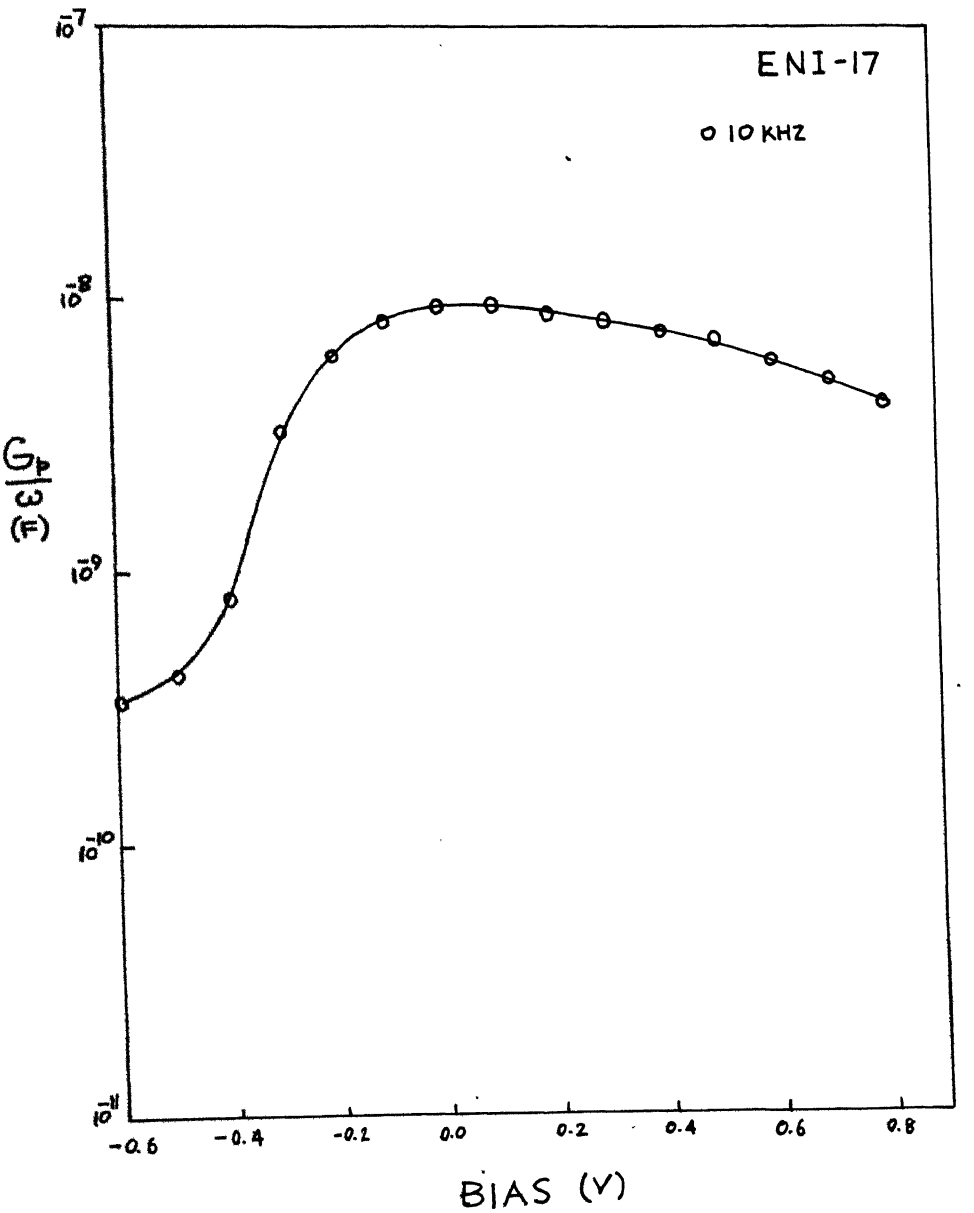

ENI-17
0 10 KHZ
10^{-7}
10^{-8}
10^{-9}
10^{-10}
10^{-11}
$\frac{G_p}{\omega}$ (F)
-0.6
-0.4
-0.2
0.0
0.2
0.4
0.6
0.8
BIAS (V)

FIG. 3.17

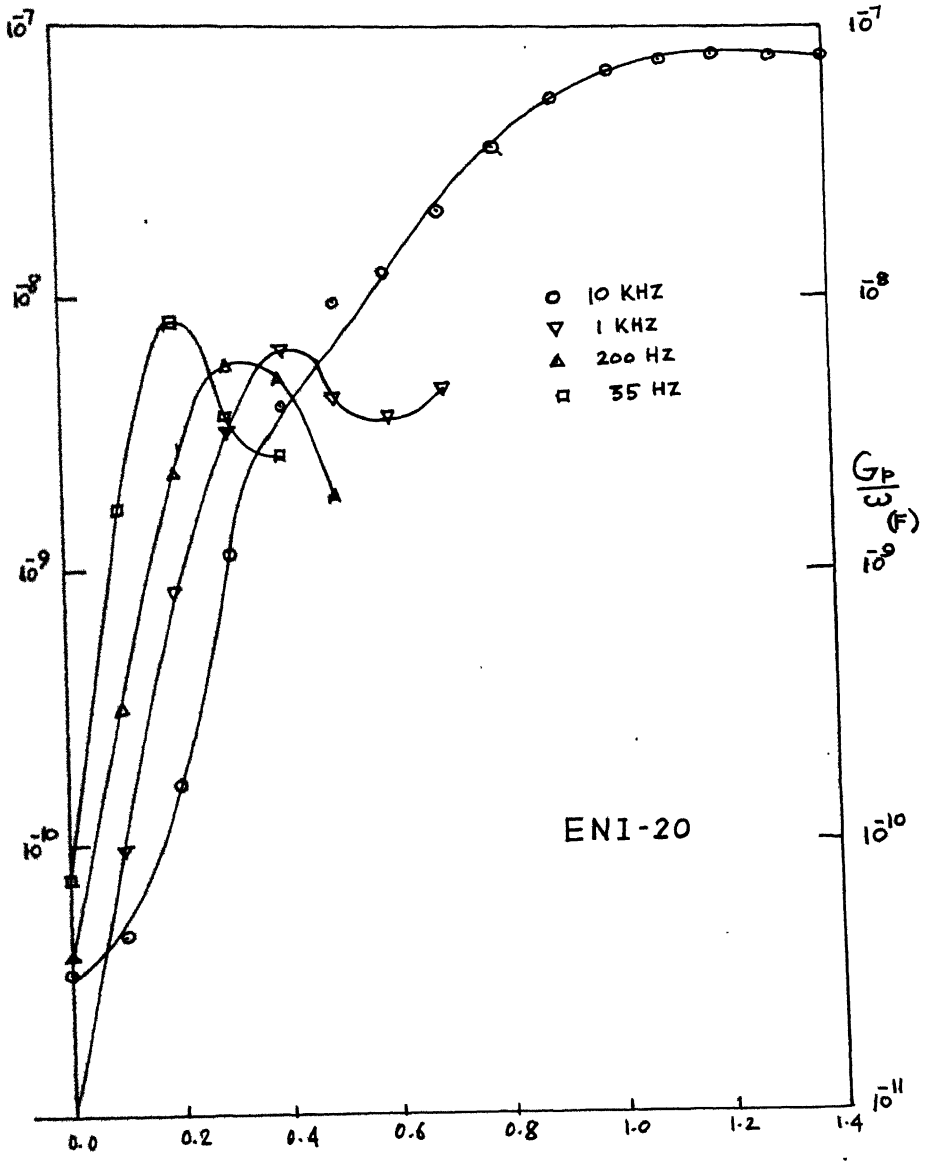

10 KHZ
1 KHZ
200 HZ
35 HZ
ENI-20
BIAS (V)
0.0
0.2
0.4
0.6
0.8
1.0
1.2
1.4
$\frac{G_p}{\omega}$ (F)

Fig. 3.18

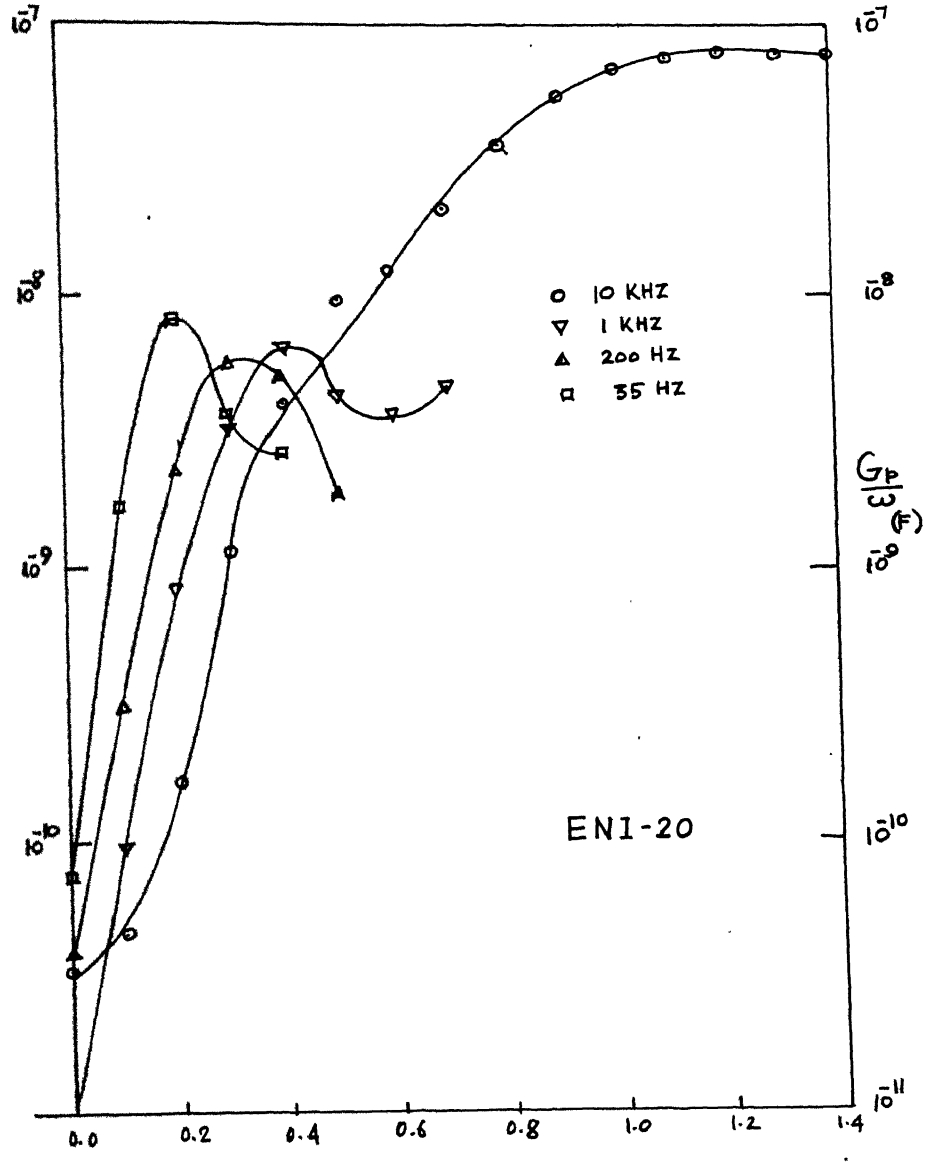

10 KHZ
1 KHZ
200 HZ
35 HZ
ENI-20
0.0
0.2
0.4
0.6
0.8
1.0
1.2
1.4
BIAS (V)
$\frac{G_p}{\omega}$ (F)

Fig. 3.18

If the states are so close to each other that a continuum of states exist, G_p/w goes through a maximum, when $w = 1.98$ and the peak value of (G_p/w) is given as [9]

$$\left(\frac{G_p}{w}\right)_{max.} = \frac{q\,A\,N_{is}}{2} \cdot 0.805$$

and N_{is} and τ are given by relations

(a) $$N_{is} = 1.25\ 2\left(\frac{G_p}{w}\right)_{max.} / q.A \qquad 3.15$$

(b) $$\tau = 1.98/w$$

In case of continuum under the influence of statistical fluctuations in surface potential, $w\tau = 2.5$ and N_{is} is given by relation [9]

(a) $$N_{is} = \frac{1}{C}\ \frac{2(G_p/w)_{max.}}{q.A} \qquad 3.16$$

where $0.3 < C < 0.8$. The value of C depends on surface potential and

(b) $$= 2.5/w$$

The energy location of interface states is to be determined next. Assuming that the capture cross-section for holes and electrons is independent of energy, and states exchange charge with majority carrier band,

$$E - E_v = E_g - q(\phi_n - \Psi_i^{peak}) \qquad 3.17$$

For electron exchange, nSi

The plots of N_{is} versus $E - E_v$ are obtained, as shown in Figures 3.19 for the samples ENI 17 and ENI 20.

3.3.3 Analysis of I-V Curves

The current-voltage characteristics shown in Figures 3.11 and 3.12 have been used for calculating $G_{d.c.}$ as explained in conductance analysis.

The ideality factor 'n' and zero bias current I_o were also determined from ln I - V characteristics. Though, they do not have direct use for determination of N_{is}. They were helpful in explaining behaviour of devices. For thermionic emission as dominant mode of carrier transport

$$I = I_o \left[\exp\left(\frac{qv}{nkT}\right) - 1\right] \qquad 3.18$$

giving value of

$$n = \frac{q}{kT} \frac{\partial v}{\partial(\ln I)}$$

By fitting the linear portion of ln I_F - V characteristic to the above relation, n was determined. I_o was found from the zero bias intercept on the current axis, by extrapolating the ln I_F - V curve.

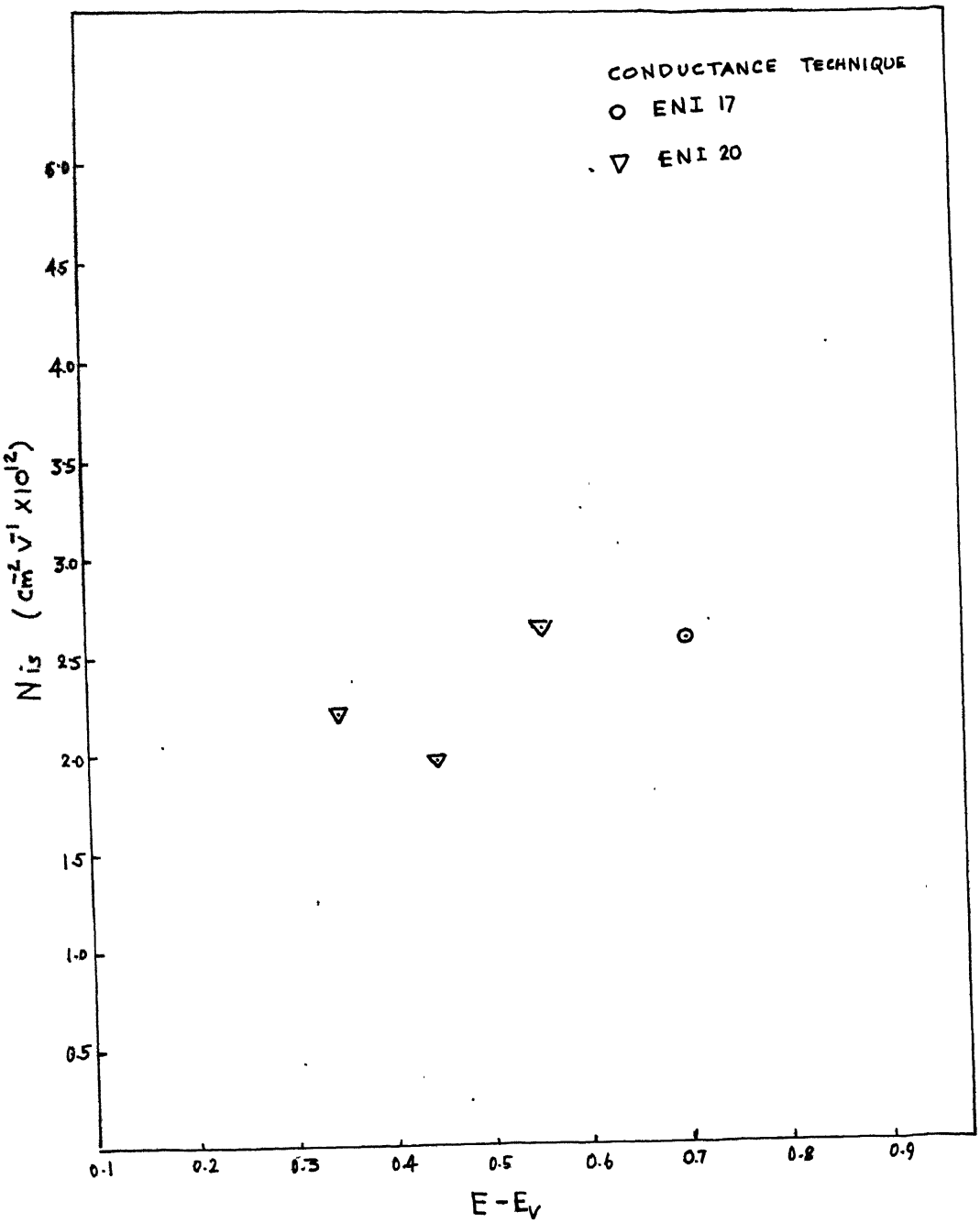

CONDUCTANCE TECHNIQUE
ENI 17
ENI 20
N_{is} ($cm^{-2} V^{-1} \times 10^{12}$)
5.0
4.5
4.0
3.5
3.0
2.5
2.0
1.5
1.0
0.5
0.1
0.2
0.3
0.4
0.5
0.6
0.7
0.8
0.9
$E - E_V$

Fig. 3.19

CHAPTER 4

RESULTS AND DISCUSSIONS

4.1 The $1/C^2$ - V characteristics (for reverse bias) in frequency range upto 10 KHz are shown in Figures 3.3 and 3.4 for unannealed ENI 17 and annealed ENI 20 samples, respectively. The zero bias surface potentials as determined by extrapolating intercept of the curve on the voltage axis were 0.201 volt for ENI 17 and 0.626 volt for ENI 20. Table 4.1 contains the experimental values of doping density, the bulk Fermi potential, the zero bias surface potential and surface barrier height.

It is observed that barrier height has remarkably increased by 0.425 volts after annealing in ENI 20 over ENI 17. This increase indicates a corresponding reduction of the oxide potential.

Finetti et.al. [24], have studied annealing of TiN/Si contacts prepared by d.c. sputtering. It has been found that the barrier height increases slightly with sequential anneal under vacuum. It has been assumed that donor like traps are created at the interface due to radiation present during sputtering process. The thermal treatment partially anneals out the traps and as a result barrier height is increased.

Pan et.al. [47] studied the electrical characteristics of the reactively RF sputtered HfN contacts. On

TABLE T.1 . RESULTS

SAMPLE	DOPING-DENSITY N_D (cm^{-3})	FERMI POTENTIAL ϕ_F (V)	ZERO BIAS SURFACE POTENTIAL ψ_i° (V)	BARRIER HEIGHT ϕ_B (V)	INTERFACE STATES DENSITY N_{is}^{MIDGAP} ($cm^{-2}\,V^{-1}$)
ENI-17	6.0×10^{15}	0.219	0.20	0.42	3.1×10^{12}
ENI-20	5.5×10^{15}	0.221	0.62	0.84	1.7×10^{12}

sequential annealing at 300, 400, 500 and 600°C for 15 minutes in a vacuum furnace, the barrier height increased slightly in nSi, which is explained by assuming that thermal treatment anneals out radiation damage introduced during sputtering process..

Various other studies [25, 26, 48] have observed that, as radiation damage anneals out, barrier height increases by small amounts.

4.2 The capacitance-voltage characteristics, for the sample ENI 17 in the frequency range of 200 Hz to 10 KHz and for the sample ENI 20 in the frequency range of 35 Hz to 10 KHz are shown in Figures 3.1 and 3.2, respectively. As expected, inversion is not observed for ENI 17. However, a dispersion of C-V is noticed.

The oxide thickness, t_{ox}, as estimated from oxidation parameters was 25 Å. For the annealed sample ENI 20, where measured capacitance tends to saturate, accurate determination of t_{ox} was done by matching slope of $\ln C_{sc}$ versus Ψ_i, and $\ln C_p$ versus Ψ_i plots in strong accumulation cf. Figure 3.6. The value of t_{ox} was determined to be 48 Å.

It is noticed, that samples though prepared under same process conditions have different oxide thickness for annealed and unannealed conditions. A similar observation [50] has been made in Si/ITO heterojunctions, annealed in N_2 at temperature larger than 600°C.

As observed by Hamasaki [51], E-beam damage of Si/SiO_2 interface is irreversible and N_{is} is not much affected at lower t_{ox}. However, the study involved structures, having 400-1600 Å thick oxides.

Kwan et.al. [25] have studied ion beam damage. By using different ion beam energies in their process, they have observed that full recovery due to ion beam damage is not possible. For higher ion beam energies, the damage is seen as donor type traps. They have concluded that interface damage for lower ion beam energies, viz. 100 eV could be annealed as damage is close to surface. For higher ion beam energies, the damage is extensive and annealing may lead to deterioration of devices.

Finetti et.al. [24], as cited earlier, have observed that sputtering damage assumes donor like traps and thermal treatment only partially anneals out interface traps, whereas, Pan et.al. [47], who used reactive RF sputtering and carried out vacuum anneal have concluded that sputtering process causes donor type traps and density of these traps vanishes after annealing.

Yet, in another study, by Schmitz et.al. [21] of radiation induced electron traps in SiO_2, where tungsten filament evaporated devices were exposed to X-ray radiation and post metallization annealing under N_2/450°C was carried out, complete recovery of damage was not observed. It was attributed to neutral traps, which do not get annealed, till >600°C temperatures are used for annealing.

4.3 The interface state density was obtained as a function of energy both by capacitance as well as conductance method.

As obtained from capacitance analysis, the Figures 3.9 and 3.10 show N_{is} distribution with energy $(E - E_v)$ for samples ENI 17 and ENI 20, respectively. The density of interface states obtained were

N_{is}^{Midgap}	ENI 17	3.1×10^{12} cm^{-2} v^{-1}
	ENI 20	1.7×10^{12} cm^{-2} v^{-1}

From the above results, we notice that density of interface states at midgap of silicon reduces to 1.7×10^{12} cm^{-2} v^{-1} from 3.1×10^{12} cm^{-2} v^{-1}, due to annealing.

The plots of interface state density as obtained from conductance technique have been shown in Figure 3.19 for the samples ENI 17 and ENI 20. The values of N_{is} obtained are close to values of N_{is} obtained both for unannealed and annealed samples from the capacitance technique. Thus results obtained by conductance technique support to those obtained from capacitance technique.

The reduction of interface state density by annealing, though substantial, it may as well be partial.

Auret et.al. [52] have also observed that ion beam sputters damage, does not get completely annealed out at temperature 500°C.

Most of the above discussions, favour the argument that annealing only partially recovers the radiation damage. Thus, the reduction in N_{is}, the interface state density, at best could be partial.

The argument is further strengthened, if we consider the observation made here viz. growth of SiO_2 layer. As determined analytically, t_{ox} does grow to 48 Å from 25 Å, due to annealing. If we consider this larger t_{ox}, we come inevitably to lower barrier height, as larger t_{ox} would mean larger V_{ox} and lower barrier height. But on the contrary, here, barrier height increases 0.425 V, irrespective of t_{ox}. The increase in t_{ox} would lead to lower interface states by itself, which supports the conclusion that role of annealing in reduction of interface states may be partial only.

Now, reverting back to the vital question of large increase of barrier height, noticed here to be 0.425 V alongwith increase in t_{ox}. In earlier studies, [51, 24, 52, 25, 47, 21] cited above, increase in barrier height observed was either small or insignificant. The reason for such observation, as against observation in this study, viz. much larger increase in barrier height could be as following. Firstly, the annealing condition and ambient used here, 500°C N_2/H_2 may have contributed

to this as against various annealing conditions employed by the earlier studies. Secondly, the structures employed for the studies earlier and this study are substantially different, and as such silicon/ITO heterojunctions with $20 < t_{ox} < 40$ Å, may be anticipated to behave differently. As described earlier, the Si/SiO_2 interface and the oxide interfacial contains fixed charge Q_F. It seems that annealing is modifying the charges at the interface and the oxide layer, in as much, as reduction in Q_F and making trapped holes in the interfacial mobile. Thus reducing the positive charge at the interface. This obviously leads to higher barrier height.

Following charge analysis at the interface shows as to how Q_F, the fixed oxide charge which is positive in nature is getting reduced.

By referring to Figure 2.2, at zero bias i.e. $V = 0$, the silicon band bending Ψ_i^o may be written as

$$\Psi_i^o = \frac{1}{q}(X^{ITO} - X^{Si}) - (\phi_n + \phi_n^{ITO} + V_{ox}^o) \qquad 4.1$$

$$\text{and } [\Psi_i^o]_1 = \frac{1}{q}(X^{ITO} - X^{Si}) - (\phi_n + \phi_n^{ITO} + V_{ox\ 1}^o) \qquad 4.2$$

$$[\Psi_i^o]_2 = \frac{1}{q}(X^{ITO} - X^{Si}) - (\phi_n + \phi_n^{ITO} + V_{ox\ 2}^o)$$

where suffixes o refer to zero bias condition

1 refer to unannealed sample ENI 17

2 refer to annealed sample ENI 20

Such that

$$\Delta\Psi_i^o = [\Psi_i^o]_2 - [\Psi_i^o]_1 = -(0.62 - 0.20) = -0.42 \text{ V}$$

or $$\Delta\Psi_i^o = -([V_{ox}^o]_2 - [V_{ox}^o]_1) = -0.42 \text{ V} \qquad 4.3$$

Now, we may also write:

$$V_{ox}^o = -\frac{Q_{sc}^o + Q_F + Q_{is}^o}{C_{ox}}$$

$$\simeq -\frac{Q_F + Q_{is}^o}{C_{ox}} \qquad \text{since } Q_{sc}^o << Q_F + Q_{is}^o \qquad 4.4$$

and from equation 4.4, for our case

$$[V_{ox}^o]_1 = -\frac{[Q_F]_1 + [Q_{is}^o]_1}{[C_{ox}]_1} \qquad 4.5$$

and $$[V_{ox}^o]_2 = -\frac{[Q_F]_2 + [Q_{is}^o]_2}{[C_{ox}]_2} \qquad 4.6$$

Thus change in V_{ox}^o from the unannealed case to annealed case from equations 4.5 and 4.6 is

$$\Delta V_{ox}^o = [V_{ox}^o]_1 - [V_{ox}^o]_2$$

$$= -\frac{[Q_F]_1}{[C_{ox}]_1} - \frac{[Q_{is}^o]_1}{[C_{ox}]_1} + \frac{[Q_F]_2}{[C_{ox}]_2} + \frac{[Q_{is}^o]_2}{[C_{ox}]_2}$$

$$= \frac{[Q_F]_2}{[C_{ox}]_2} - \frac{[Q_F]_1}{[C_{ox}]_1} + \frac{[Q_{is}^o]_2}{[C_{ox}]_2} - \frac{[Q_{is}^o]_1}{[C_{ox}]_1} \qquad 4.7$$

To evaluate ΔV^{o}_{ox}, its nature and value we determine $\frac{[Q^{o}_{is}]_2}{[C_{ox}]_2} - \frac{[Q^{o}_{is}]_1}{[C_{ox}]_1}$ as following:

We know, in general, the interface state charge may be written as,

$$Q^{o}_{is} = q \int_{E_F}^{E_C} N^{D}_{is} \cdot dE - q \int_{E_V}^{E_F} N^{A}_{is} \cdot dE \qquad 4.8$$

where N^{D}_{is} = Donor type interface states density

N^{A}_{is} = Acceptor type interface states density.

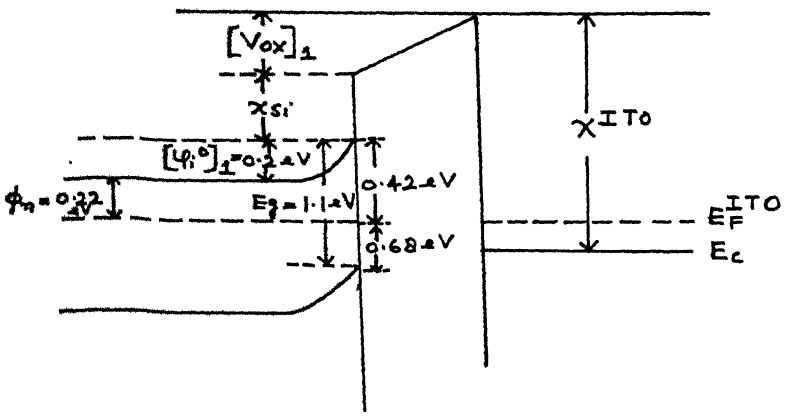
Writing equation 4. for our situation. For limits of integration cf. Figures 4.1(a) and 4.1(b)

$$[Q^{o}_{is}]_1 = q \int_{E_V + 0.68\ eV}^{E_C} [N^{D}_{is}]_1 \cdot dE - q \int_{E_V}^{E_V + 0.68\ eV} [N^{A}_{is}]_1 \cdot dE \qquad 4.9$$

$$[Q^{o}_{is}]_2 = q \int_{E_V + 0.26\ eV}^{E_C} [N^{D}_{is}]_2 \cdot dE - q \int_{E_V}^{E_V + 0.26\ eV} [N^{A}_{is}]_2 \cdot dE \qquad 4.10$$

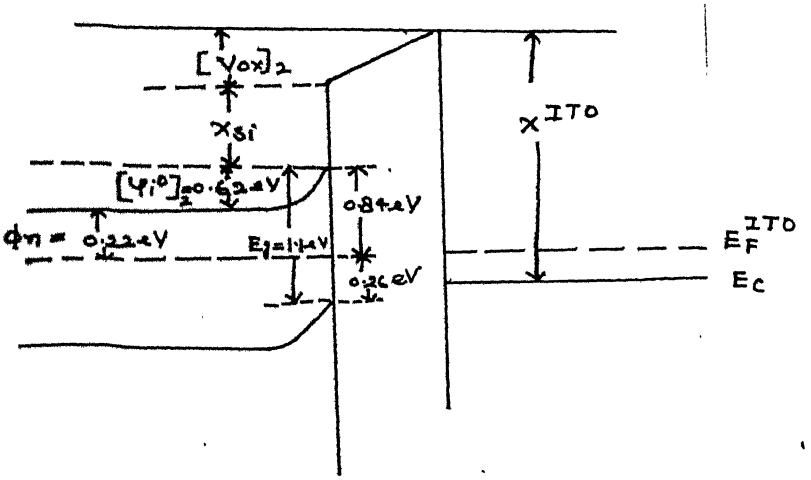
From equations 4.9 and 4.10,

$$\begin{aligned} \frac{[Q^{o}_{is}]_2}{[C_{ox}]_2} - \frac{[Q^{o}_{is}]_1}{[C_{ox}]_1} = {} & \frac{q}{[C_{ox}]_2} \int_{E_V + 0.26\ eV}^{E_C} [N^{D}_{is}]_2 \cdot dE \\ & - \frac{q}{[C_{ox}]_1} \int_{E_V + 0.68\ eV}^{E_C} [N^{D}_{is}]_1 \cdot dE \\ & + \frac{q}{[C_{ox}]_1} \int_{E_V}^{E_V + 0.68\ eV} [N^{A}_{is}]_1 \cdot dE \\ & - \frac{q}{[C_{ox}]_2} \int_{E_V}^{E_V + 0.26\ eV} [N^{A}_{is}]_1 \cdot dE \end{aligned} \qquad 4.11$$



SAMPLE ENI-17

(a)



SAMPLE ENI-20

(b)

Fig. 4.1(a) : Energy Band diagram of sample ENI-17 unannealed case

(b) : Energy Band diagram of sample ENI-20 annealed under 500°C, $N_2|H_2$

Using following relationships and values as determined in our case,

$$[C_{ox}]_1 \simeq 2[C_{ox}]_2 \qquad \text{Since } [t_{ox}]_2 \simeq 2[t_{ox}]_1$$

$$[t_{ox}]_2 = 48 \text{ Å}$$

$$[t_{ox}]_1 = 25 \text{ Å}$$

and $[N_{is}]_1 \simeq 2[N_{is}]_2$ Since $[N_{is}]_1 = 3.1 \times 10^{12} \text{ cm}^{-2}\text{v}^{-1}$

$$[N_{is}]_2 = 1.7 \times 10^{12} \text{ cm}^{-2}\text{v}^{-1}$$

in equation 4.11, we get

$$\frac{[Q_{is}]_2}{[C_{ox}]_2} - \frac{[Q_{is}]_1}{[C_{ox}]_1} - \frac{q}{[C_{ox}]_2} \int_{E_V + 0.26 \text{ eV}}^{E_V + 0.68 \text{ eV}} [N_{is}]_2 \cdot dE \qquad 4.12$$

By using experimental values and their extrapolations, we get,

$$\frac{[Q_{is}]_2}{[C_{ox}]_2} - \frac{[Q_{is}]_1}{[C_{ox}]_1} \simeq \frac{q \times 2.0 \times 10^{12} \times (0.68 - 0.26)}{53 \times 10^{-9}/7.52 \times 10^{-2}}$$

$$\simeq 0.2 \text{ V}$$

Now, substituting the value of above expression in equation 4.7, we get

$$\Delta V_{ox}^{o} = \frac{[Q_F]_2}{[C_{ox}]_2} - \frac{[Q_F]_1}{[C_{ox}]_1} + 0.2 \text{ V} = -0.42 \text{ V}$$

and $$\frac{[Q_F]_2}{[C_{ox}]_2} - \frac{[Q_F]_1}{[C_{ox}]_1} = (-0.42 - 0.20) \text{ V} = -0.62 \text{ V}$$

Thus we notice, that nature of change of Q_F is a negative quantity. This leads to inevitable conclusion that fixed

positive charge Q_F is reducing at the interface.

To sum up the argument, it may be said that large increase in barrier height due to annealing, not noticed hitherto is more due to a reduction in Q_F than in Q_{is}.

CHAPTER 5

CONCLUSION

The characterisation for the interface states in Si/ITO heterojunctions annealed under 500°C N_2/H_2 has been done by the capacitance as well as conductance techniques, in dark, at room temperature.

Based on the measured capacitance-voltage and conductance voltage data and the analysis carried on relating to above techniques, it has been found that reduction in interface state density has not been very significant. However an increase in the oxide layer has been noticed due to annealing. Also, a large increase of barrier height in annealed sample over unannealed sample has been noticed. On analysing charges at the interface, it has been found that Q_F, the fixed oxide charge, which has positive nature, reduces due to annealing. Thus, reason for increase of such large barrier height may be due to reduction of fixed oxide charge at the interface. No earlier study, in such structures has made any observations in reference to effect of annealing on interface oxide charges. In thick oxide structures, improvements in radiation damage due to annealing, in respect of interface state density have been noticed. In the present study, it is concluded that in case of Si/ITO structures having thin interfacial $t_{ox} < 40$ Å, a large increase in barrier height noticed due to annealing, is explained as more due to reduction of positive fixed charge Q_F than reduction of Q_{is} or N_{is}.

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